

SN74LVC1G66 Single Bilateral Analog Switch

1 Features

- Available in the Texas Instruments NanoFree™ Package
- 1.65-V to 5.5-V V_{CC} Operation
- Inputs Accept Voltages to 5.5 V
- Max t_{pd} of 0.8 ns at 3.3 V
- High On-Off Output Voltage Ratio
- High Degree of Linearity
- High Speed, Typically 0.5 ns ($V_{CC} = 3$ V, $C_L = 50$ pF)
- Low ON-State Resistance, Typically $\approx 5.5 \Omega$ ($V_{CC} = 4.5$ V)
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

2 Applications

- Wireless Devices
- Audio and Video Signal Routing
- Portable Computing
- Wearable Devices
- Signal Gating, Chopping, Modulation or Demodulation (Modem)
- Signal Multiplexing for Analog-to-Digital and Digital-to-Analog Conversion Systems

3 Description

This single analog switch is designed for 1.65-V to 5.5-V V_{CC} operation.

The SN74LVC1G66 device can handle analog and digital signals. The device permits bidirectional transmission of signals with amplitudes of up to 5.5 V (peak).

NanoFree package technology is a major breakthrough in IC packaging concepts, using the die as the package.

Device Information⁽¹⁾

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|----------------|------------|-------------------|
| SN74LVC1G66DBV | SOT-23 (5) | 2.90 mm × 1.60 mm |
| SN74LVC1G66DCK | SC70 (5) | 2.00 mm × 1.25 mm |
| SN74LVC1G66DRL | SOT (5) | 1.60 mm × 1.20 mm |
| SN74LVC1G66DRY | SON (6) | 1.45 mm × 1.00 mm |
| SN74LVC1G66YZP | DSBGA (5) | 1.39 mm × 0.89 mm |
| SN74LVC1G66DSF | SON (6) | 1.00 mm × 1.00 mm |

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Logic Diagram (Positive Logic)

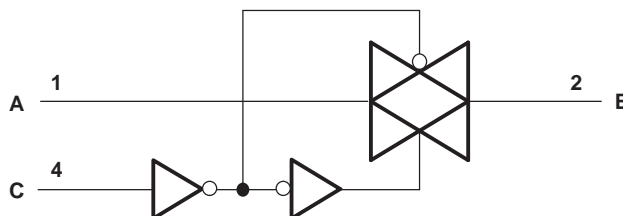


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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision P (March 2016) to Revision Q Page

- Changed the YZP package pin out graphic..... **4**

Changes from Revision O (March 2015) to Revision P Page

- Added Junction temperature spec to *Absolute Maximum Ratings* table **5**
- Added "Control" to "Input transition rise and fall time" in *Recommended Operating Conditions* table **5**

Changes from Revision N (December 2012) to Revision O Page

- Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section **1**
- Removed *Ordering Information* table **1**
- Added *Device Information* table **1**

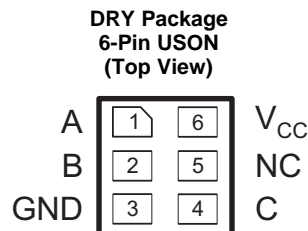
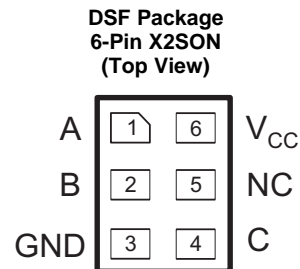
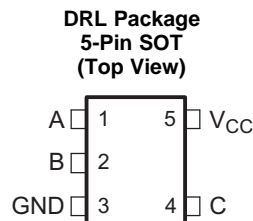
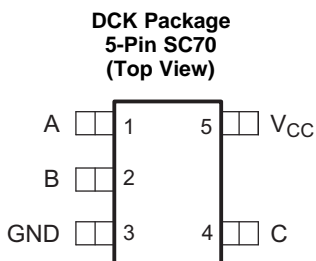
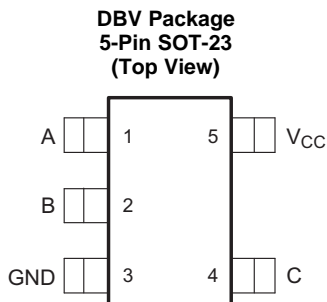
Changes from Revision M (January 2012) to Revision N Page

- Added jumbo reel to *Ordering Information* table **1**

Changes from Revision L (January 2007) to Revision M Page

- Added DSF and DRY package to pin out graphic..... **3**

5 Pin Configuration and Functions

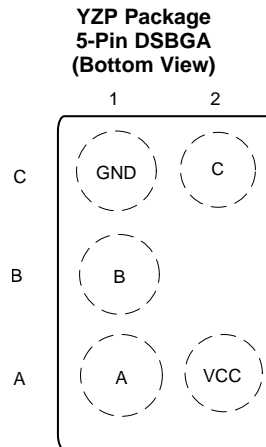


Pin Functions

| PIN | | | I/O | DESCRIPTION |
|-----------------|---------|-----------------|-----|---------------------------------------|
| NAME | SOT NO. | USON, X2SON NO. | | |
| A | 1 | 1 | I/O | Bidirectional signal to be switched |
| B | 2 | 2 | I/O | Bidirectional signal to be switched |
| C | 4 | 4 | I | Controls the switch (L = OFF, H = ON) |
| GND | 3 | 3 | — | Ground pin |
| NC | — | 5 | — | Do not connect |
| V _{CC} | 5 | 6 | — | Power pin |

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Pin Functions

| PIN | | I/O | DESCRIPTION |
|-----------------|-----------|-----|---------------------------------------|
| NAME | DSBGA NO. | | |
| A | A1 | I/O | Bidirectional signal to be switched |
| B | B1 | I/O | Bidirectional signal to be switched |
| C | C2 | I | Controls the switch (L = OFF, H = ON) |
| GND | C1 | — | Ground pin |
| V _{CC} | A2 | — | Power pin |

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

| | | MIN | MAX | UNIT |
|------------------|---|--|-----------------------|------|
| V _{CC} | Supply voltage ⁽²⁾ | –0.5 | 6.5 | V |
| V _I | Input voltage ⁽²⁾⁽³⁾ | –0.5 | 6.5 | V |
| V _{I/O} | Switch I/O voltage ⁽²⁾⁽³⁾⁽⁴⁾ | –0.5 | V _{CC} + 0.5 | V |
| I _{IK} | Control input clamp current | V _I < 0 | –50 | mA |
| I _{I/O} | I/O port diode current | V _{I/O} < 0 or V _{I/O} > V _{CC} | ±50 | mA |
| I _T | ON-state switch current | V _{I/O} < 0 to V _{CC} | ±50 | mA |
| | Continuous current through V _{CC} or GND | | ±100 | mA |
| T _{stg} | Storage Temperature | –65 | 150 | °C |
| T _j | Junction Temperature | | 150 | °C |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages are with respect to ground, unless otherwise specified.
- (3) The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
- (4) This value is limited to 5.5 V maximum.

6.2 ESD Ratings

| | | VALUE | UNIT |
|--------------------|-------------------------|--|-------|
| V _(ESD) | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾ | +2000 |
| | | Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾ | +1000 |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

| | | MIN | MAX | UNIT |
|------------------|---|------------------------------------|------------------------|------|
| V _{CC} | Supply voltage | 1.65 | 5.5 | V |
| V _{I/O} | I/O port voltage. | 0 | V _{CC} | V |
| V _{IH} | High-level input voltage, control input | V _{CC} = 1.65 V to 1.95 V | V _{CC} × 0.65 | V |
| | | V _{CC} = 2.3 V to 2.7 V | V _{CC} × 0.7 | |
| | | V _{CC} = 3 V to 3.6 V | V _{CC} × 0.7 | |
| | | V _{CC} = 4.5 V to 5.5 V | V _{CC} × 0.7 | |
| V _{IL} | Low-level input voltage, control input | V _{CC} = 1.65 V to 1.95 V | V _{CC} × 0.35 | V |
| | | V _{CC} = 2.3 V to 2.7 V | V _{CC} × 0.3 | |
| | | V _{CC} = 3 V to 3.6 V | V _{CC} × 0.3 | |
| | | V _{CC} = 4.5 V to 5.5 V | V _{CC} × 0.3 | |
| V _I | Control input voltage | 0 | 5.5 | V |
| Δt/Δv | Control input transition rise and fall time | V _{CC} = 1.65 V to 1.95 V | 20 | ns/V |
| | | V _{CC} = 2.3 V to 2.7 V | 20 | |
| | | V _{CC} = 3 V to 3.6 V | 10 | |
| | | V _{CC} = 4.5 V to 5.5 V | 10 | |
| T _A | Operating free-air temperature | –40 | 85 | °C |

- (1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, [SCBA004](#).

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6.4 Thermal Information

| THERMAL METRIC | SN74LVC1G66 | | | | | | UNIT |
|--|-----------------|---------------|-----------|---------------|----------------|----------------|------|
| | DBV (SOT-23) | DCK (SC70) | DRL (SOT) | DRY (USON) | DSF (X2SON) | YZP (DSBGA) | |
| | 5 PINS | 5 PINS | 5 PINS | 6 PINS | 6 PINS | 5 PINS | |
| $R_{\theta JA}$ Junction-to-ambient thermal resistance | 206 | 252 | 142 | — | — | 132 | °C/W |

6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | V_{CC} | MIN | TYP ⁽¹⁾ | MAX | UNIT |
|---|--|--------------------------|--------|----------------------|-----|---------------|
| r_{on} ON-state switch resistance | $V_I = V_{CC}$ or GND, $V_C = V_{IH}$ (see Figure 2 and Figure 1) | $I_S = 4$ mA | 1.65 V | 12 | 30 | Ω |
| | | $I_S = 8$ mA | 2.3 V | 9 | 20 | |
| | | $I_S = 24$ mA | 3 V | 7.5 | 15 | |
| | | $I_S = 32$ mA | 4.5 V | 5.5 | 10 | |
| $r_{on(p)}$ Peak on resistance | $V_I = V_{CC}$ or GND, $V_C = V_{IH}$ (see Figure 2 and Figure 1) | $I_S = 4$ mA | 1.65 V | 74.5 | 120 | Ω |
| | | $I_S = 8$ mA | 2.3 V | 20 | 30 | |
| | | $I_S = 24$ mA | 3 V | 11.5 | 20 | |
| | | $I_S = 32$ mA | 4.5 V | 7.5 | 15 | |
| $I_{S(off)}$ OFF-state switch leakage current | $V_I = V_{CC}$ and $V_O =$ GND or $V_I =$ GND and $V_O = V_{CC}$, $V_C = V_{IL}$ (see Figure 3) | $T_A = 25^\circ\text{C}$ | 5.5 V | ± 1 ± 0.1 | | μA |
| $I_{S(on)}$ ON-state switch leakage current | $V_I = V_{CC}$ or GND, $V_C = V_{IH}$, $V_O =$ Open (see Figure 4) | $T_A = 25^\circ\text{C}$ | 5.5 V | ± 1 ± 0.1 | | μA |
| I_I Control input current | $V_C = V_{CC}$ or GND | $T_A = 25^\circ\text{C}$ | 5.5 V | ± 1 ± 0.1 | | μA |
| I_{CC} Supply current | $V_C = V_{CC}$ or GND | $T_A = 25^\circ\text{C}$ | 5.5 V | 10 1 | | μA |
| ΔI_{CC} Supply current change | $V_C = V_{CC} - 0.6$ V | | 5.5 V | | 500 | μA |
| C_{ic} Control input capacitance | | | 5 V | 2 | | pF |
| $C_{io(off)}$ Switch input and output capacitance | | | 5 V | 6 | | pF |
| $C_{io(on)}$ Switch input and output capacitance | | | 5 V | 13 | | pF |

(1) $T_A = 25^\circ\text{C}$

6.6 Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 5)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC} = 1.8$ V ± 0.15 V | | $V_{CC} = 2.5$ V ± 0.2 V | | $V_{CC} = 3.3$ V ± 0.3 V | | $V_{CC} = 5$ V ± 0.5 V | | UNIT |
|-----------------|-----------------|----------------|----------------------------------|-----|---------------------------------|-----|---------------------------------|-----|-------------------------------|-----|------|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $t_{pd}^{(1)}$ | A or B | B or A | | 2 | | 1.2 | | 0.8 | | 0.6 | ns |
| $t_{en}^{(2)}$ | C | A or B | 2.5 | 12 | 1.9 | 6.5 | 1.8 | 5 | 1.5 | 4.2 | ns |
| $t_{dis}^{(3)}$ | C | A or B | 2.2 | 10 | 1.4 | 6.9 | 2 | 6.5 | 1.4 | 5 | ns |

(1) t_{PLH} and t_{PHL} are the same as t_{pd} . The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

(2) t_{PZL} and t_{PZH} are the same as t_{en} .

(3) t_{PLZ} and t_{PHZ} are the same as t_{dis} .

6.7 Analog Switch Characteristics

 $T_A = 25^\circ\text{C}$

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | TEST CONDITIONS | V_{CC} | TYP | UNIT |
|--|--------------|-------------|--|----------|--------|------|
| Frequency response ⁽¹⁾ (switch ON) | A or B | B or A | $C_L = 50\text{ pF}$, $R_L = 600\ \Omega$, $f_{in} = \text{sine wave}$ (see Figure 6) | 1.65 V | 35 | MHz |
| | | | | 2.3 V | 120 | |
| | | | | 3 V | 175 | |
| | | | | 4.5 V | 195 | |
| | | | $C_L = 5\text{ pF}$, $R_L = 50\ \Omega$, $f_{in} = \text{sine wave}$ (see Figure 6) | 1.65 V | >300 | |
| | | | | 2.3 V | >300 | |
| | | | | 3 V | >300 | |
| | | | | 4.5 V | >300 | |
| Crosstalk (control input to signal output) | C | A or B | $C_L = 50\text{ pF}$, $R_L = 600\ \Omega$, $f_{in} = 1\text{ MHz}$ (square wave) (see Figure 7) | 1.65 V | 35 | mV |
| | | | | 2.3 V | 50 | |
| | | | | 3 V | 70 | |
| | | | | 4.5 V | 100 | |
| Feedthrough attenuation ⁽²⁾ (switch OFF) | A or B | B or A | $C_L = 50\text{ pF}$, $R_L = 600\ \Omega$, $f_{in} = 1\text{ MHz}$ (sine wave) (see Figure 8) | 1.65 V | –58 | dB |
| | | | | 2.3 V | –58 | |
| | | | | 3 V | –58 | |
| | | | | 4.5 V | –58 | |
| | | | $C_L = 5\text{ pF}$, $R_L = 50\ \Omega$, $f_{in} = 1\text{ MHz}$ (sine wave) (see Figure 8) | 1.65 V | –42 | |
| | | | | 2.3 V | –42 | |
| | | | | 3 V | –42 | |
| | | | | 4.5 V | –42 | |
| Sine-wave distortion | A or B | B or A | $C_L = 50\text{ pF}$, $R_L = 10\text{ k}\Omega$, $f_{in} = 1\text{ kHz}$ (sine wave) (see Figure 9) | 1.65 V | 0.1% | |
| | | | | 2.3 V | 0.025% | |
| | | | | 3 V | 0.015% | |
| | | | | 4.5 V | 0.01% | |
| | | | $C_L = 50\text{ pF}$, $R_L = 10\text{ k}\Omega$, $f_{in} = 10\text{ kHz}$ (sine wave) (see Figure 9) | 1.65 V | 0.15% | |
| | | | | 2.3 V | 0.025% | |
| | | | | 3 V | 0.015% | |
| | | | | 4.5 V | 0.01% | |

(1) Adjust f_{in} voltage to obtain 0 dBm at output. Increase f_{in} frequency until dB meter reads –3 dB.

(2) Adjust f_{in} voltage to obtain 0 dBm at input.

6.8 Operating Characteristics

 $T_A = 25^\circ\text{C}$

| PARAMETER | TEST CONDITIONS | $V_{CC} = 1.8\text{ V}$ | $V_{CC} = 2.5\text{ V}$ | $V_{CC} = 3.3\text{ V}$ | $V_{CC} = 5\text{ V}$ | UNIT |
|--|---------------------|-------------------------|-------------------------|-------------------------|-----------------------|------|
| | | TYP | TYP | TYP | TYP | |
| C_{pd} Power dissipation capacitance | $f = 10\text{ MHz}$ | 8 | 9 | 9 | 11 | pF |

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6.9 Typical Characteristics

$T_A = 25^\circ\text{C}$

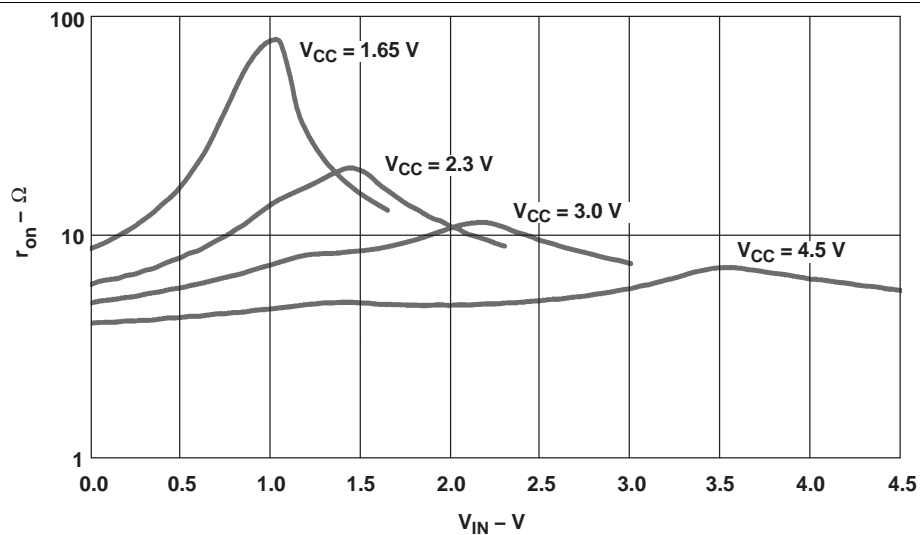


Figure 1. Typical r_{on} as a Function of Input Voltage (V_I) for $V_I = 0$ to V_{CC}

7 Parameter Measurement Information

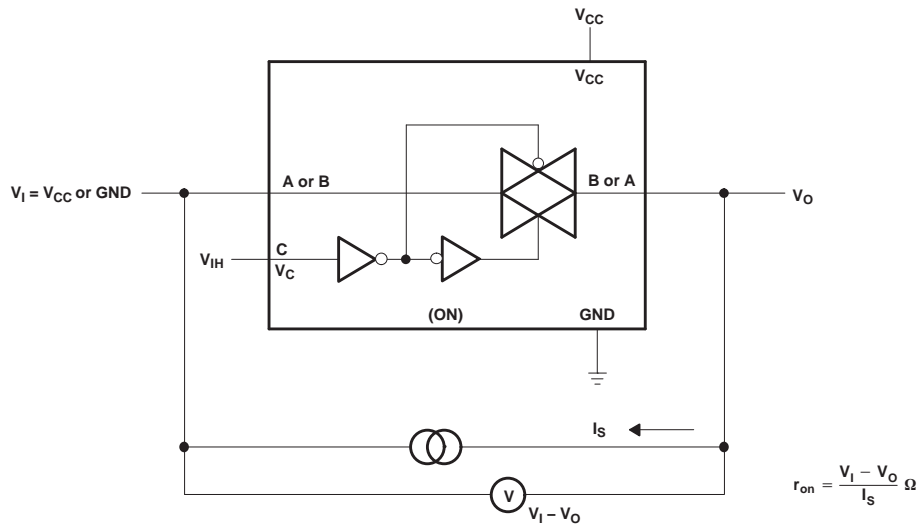


Figure 2. ON-State Resistance Test Circuit

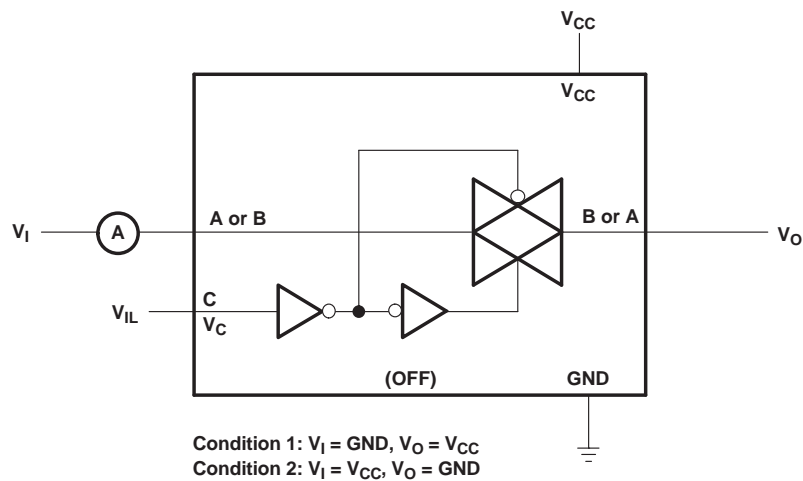


Figure 3. OFF-State Switch Leakage-Current Test Circuit

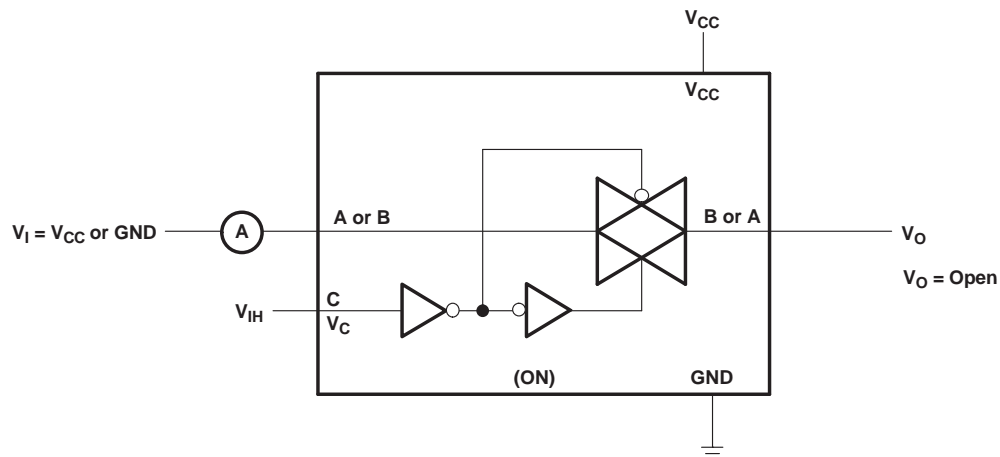
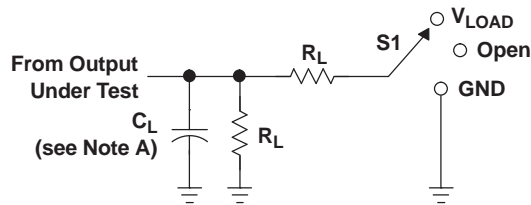


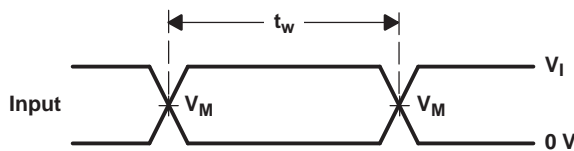
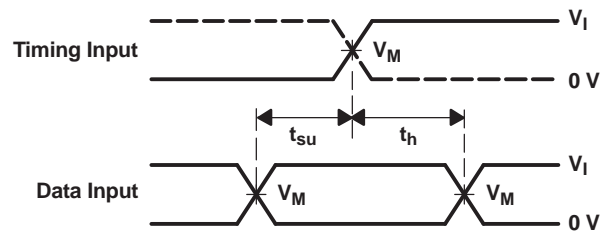
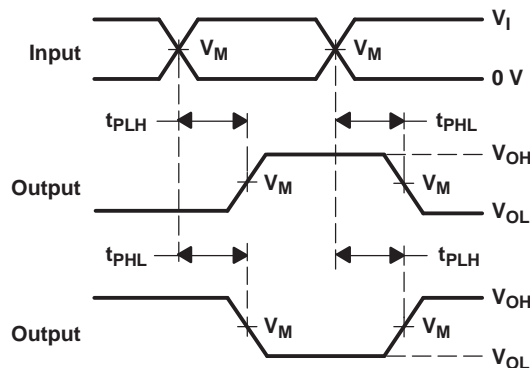
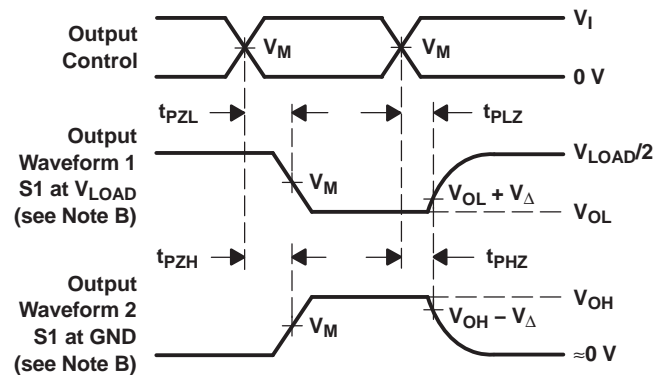
Figure 4. ON-State Switch Leakage-Current Test Circuit

Parameter Measurement Information (continued)


LOAD CIRCUIT

| TEST | S1 |
|-------------------|------------|
| t_{PLH}/t_{PHL} | Open |
| t_{PLZ}/t_{PZL} | V_{LOAD} |
| t_{PHZ}/t_{PZH} | GND |

| V_{CC} | INPUTS | | V_M | V_{LOAD} | C_L | R_L | V_{Δ} |
|----------------------------------|----------|----------------------|------------|-------------------|-------|--------------|--------------|
| | V_I | t_r/t_f | | | | | |
| $1.8\text{ V} \pm 0.15\text{ V}$ | V_{CC} | $\leq 2\text{ ns}$ | $V_{CC}/2$ | $2 \times V_{CC}$ | 30 pF | 1 k Ω | 0.15 V |
| $2.5\text{ V} \pm 0.2\text{ V}$ | V_{CC} | $\leq 2\text{ ns}$ | $V_{CC}/2$ | $2 \times V_{CC}$ | 30 pF | 500 Ω | 0.15 V |
| $3.3\text{ V} \pm 0.3\text{ V}$ | V_{CC} | $\leq 2.5\text{ ns}$ | $V_{CC}/2$ | $2 \times V_{CC}$ | 50 pF | 500 Ω | 0.3 V |
| $5\text{ V} \pm 0.5\text{ V}$ | V_{CC} | $\leq 2.5\text{ ns}$ | $V_{CC}/2$ | $2 \times V_{CC}$ | 50 pF | 500 Ω | 0.3 V |


**VOLTAGE WAVEFORMS
PULSE DURATION**

**VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES**

**VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS**

**VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING**

- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\text{ }\Omega$.
 - The outputs are measured one at a time, with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .
 - All parameters and waveforms are not applicable to all devices.

Figure 5. Load Circuit and Voltage Waveforms

Parameter Measurement Information (continued)

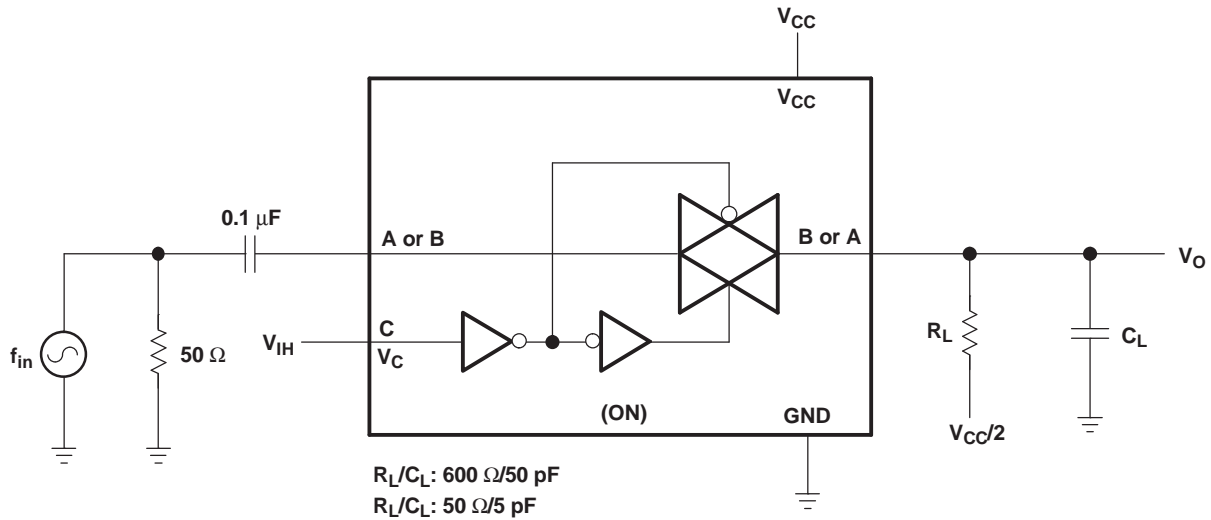


Figure 6. Frequency Response (Switch ON)

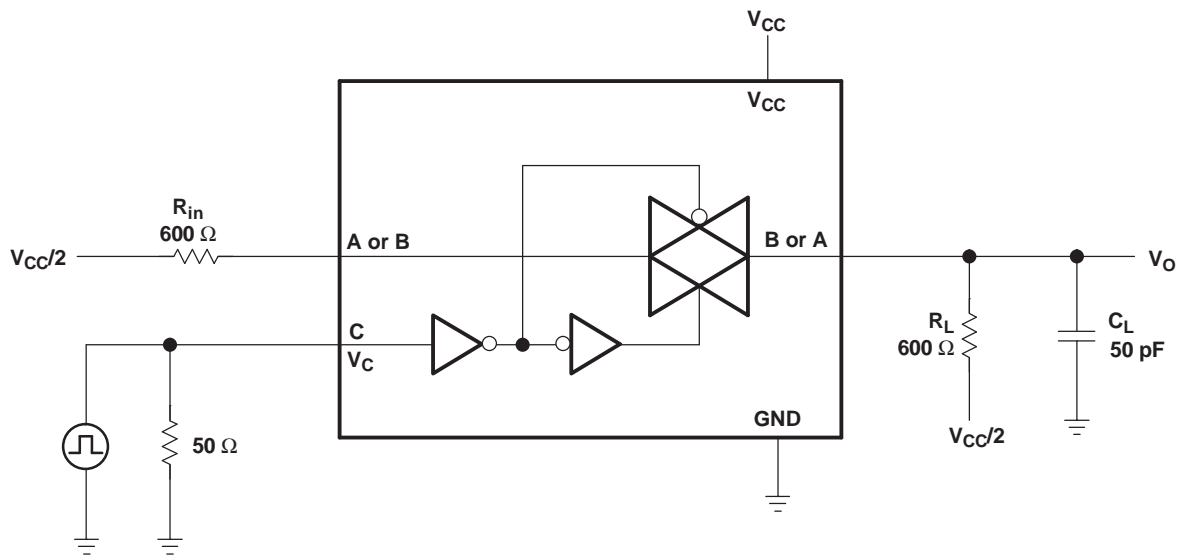


Figure 7. Crosstalk (Control Input – Switch Output)

Parameter Measurement Information (continued)

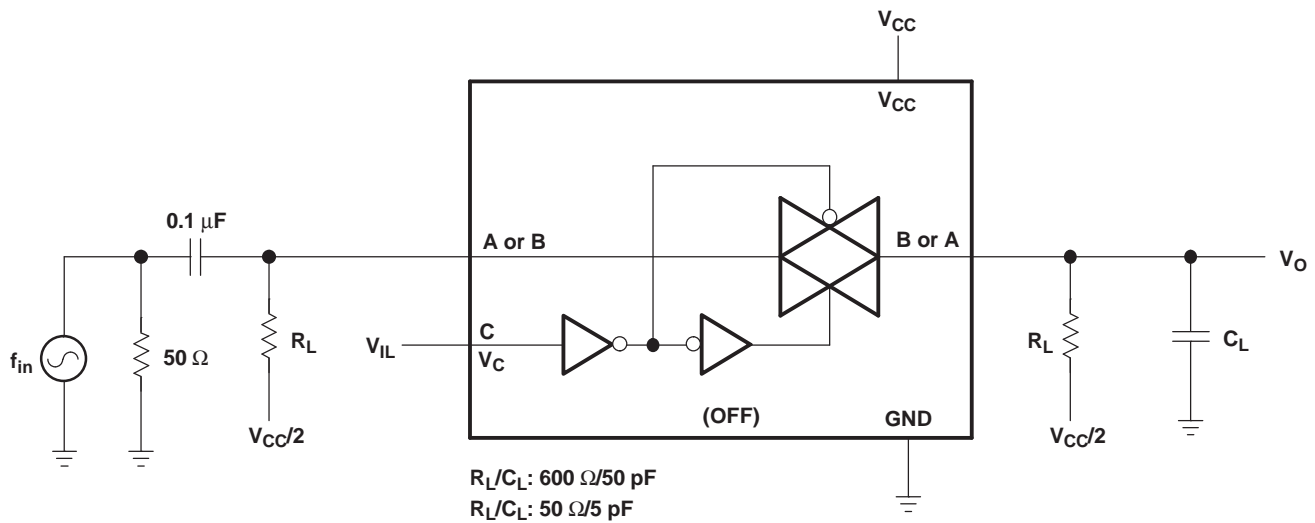


Figure 8. Feedthrough (Switch OFF)

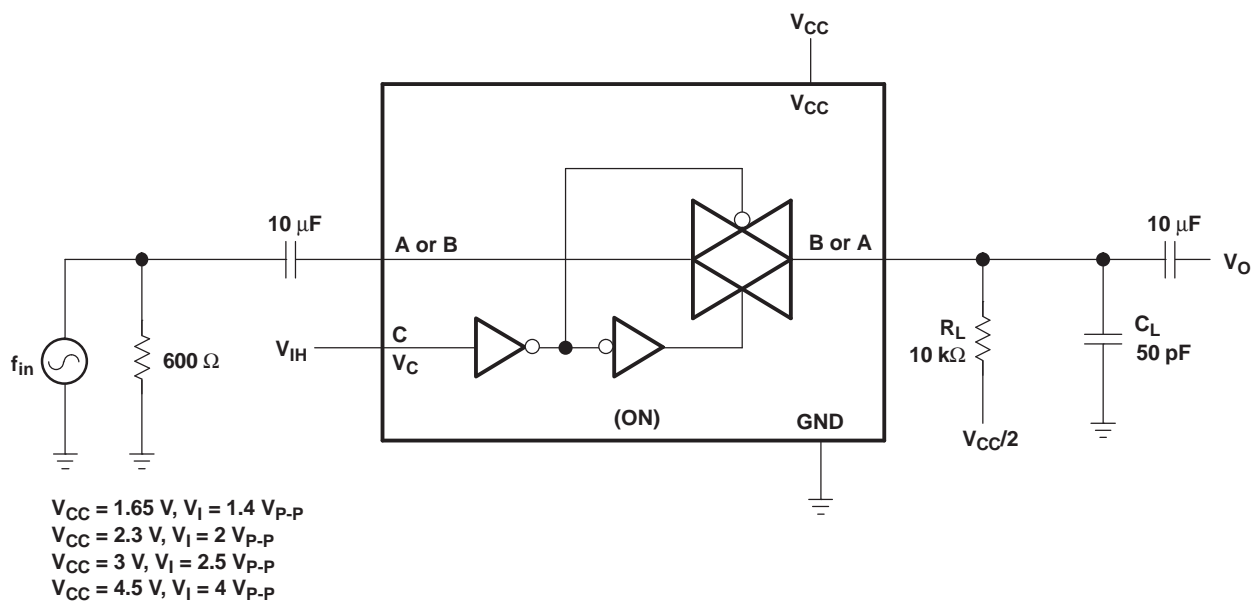


Figure 9. Sine-Wave Distortion

8 Detailed Description

8.1 Overview

This single analog switch is designed for 1.65-V to 5.5-V V_{CC} operation.

The SN74LVC1G66 device can handle analog and digital signals. The device permits bidirectional transmission of signals with amplitudes of up to 5.5 V (peak). Like all analog switches, the SN74LVC1G66 is bidirectional.

NanoFree package technology is a major breakthrough in IC packaging concepts, using the die as the package.

8.2 Functional Block Diagram

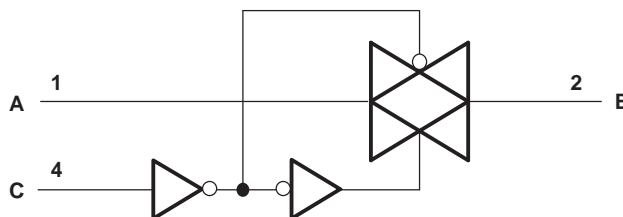


Figure 10. Logic Diagram (Positive Logic)

8.3 Feature Description

The TI NanoFree package is one of TI's smallest packages and allows customers to save board space while the solder bumps allow for easy testing. The SN74LVC1G66 has a wide V_{CC} range, allowing rail-to-rail operation of signals anywhere from a 1.8-V system to a 5-V system. In addition, the control input (C Pin) is 5.5-V tolerant, allowing higher-voltage logic to interface to the switch control system.

8.4 Device Functional Modes

Table 1. Function Table

| CONTROL INPUT (C) | SWITCH |
|-------------------|--------|
| L | OFF |
| H | ON |

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The SN74LVC1G66 can be used in any situation where an SPST switch would be used and a solid-state, voltage-controlled version is preferred.

9.2 Typical Application

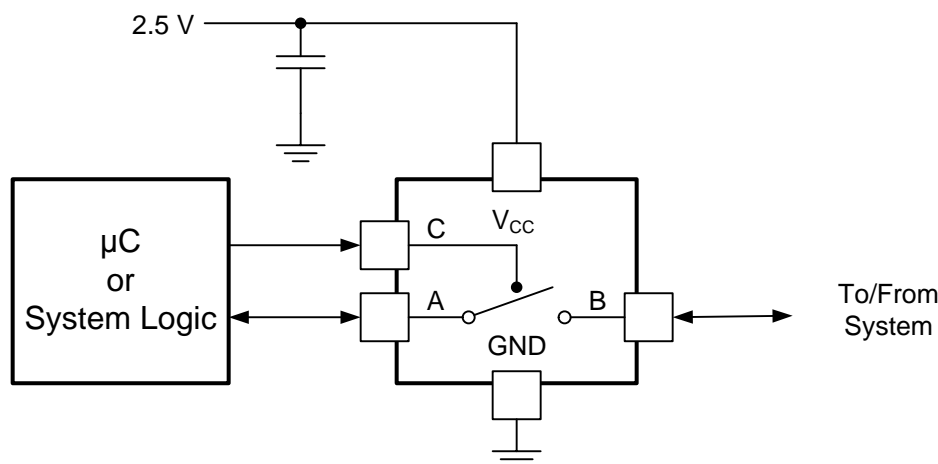


Figure 11. Typical Application Schematic

9.2.1 Design Requirements

The SN74LVC1G66 allows on and off control of analog and digital signals with a digital control signal. All input signals should remain between 0 V and V_{CC} for optimal operation.

9.2.2 Detailed Design Procedure

1. Recommended Input Conditions:
 - For rise time and fall time specifications, see $\Delta t/\Delta v$ in [Recommended Operating Conditions](#).
 - For specified high and low levels, see V_{IH} and V_{IL} in [Recommended Operating Conditions](#).
 - Inputs and outputs are overvoltage tolerant allowing them to go as high as 5.5 V at any valid V_{CC} .
2. Recommended Output Conditions:
 - Load currents should not exceed ± 50 mA.
3. Frequency Selection Criterion:
 - Maximum frequency tested is 150 MHz.
 - Added trace resistance/capacitance can reduce maximum frequency capability; use layout practices as directed in [Layout](#).

Typical Application (continued)

9.2.3 Application Curve

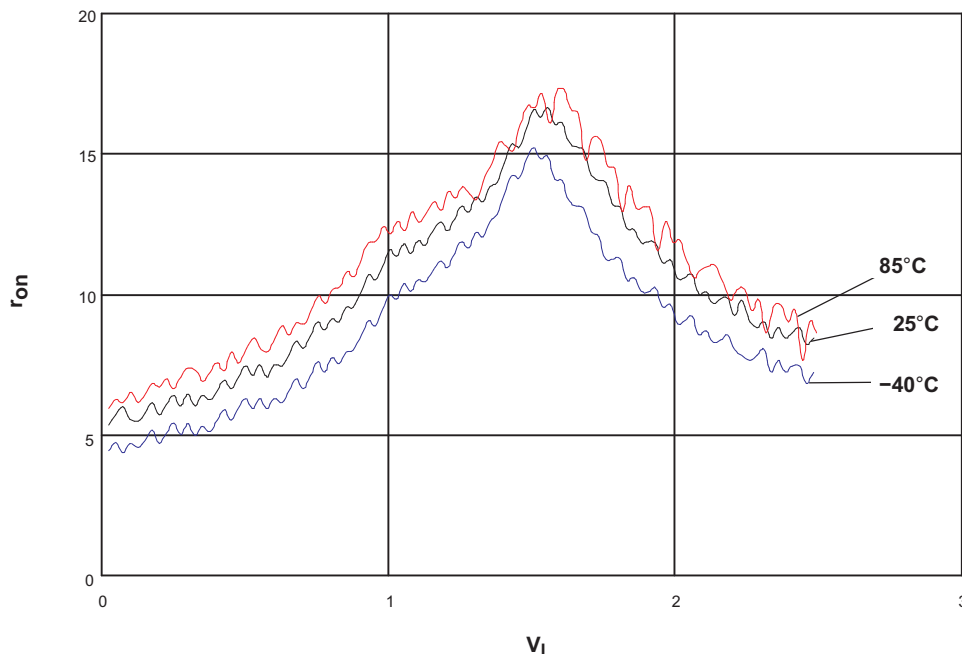


Figure 12. r_{on} vs V_I , $V_{CC} = 2.5$ V (SN74LVC1G66)

10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the [Recommended Operating Conditions](#).

Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1- μ F bypass capacitor is recommended. If there are multiple pins labeled V_{CC} , then a 0.01- μ F or 0.022- μ F capacitor is recommended for each V_{CC} because the V_{CC} pins will be tied together internally. For devices with dual supply pins operating at different voltages, for example V_{CC} and V_{DD} , a 0.1- μ F bypass capacitor is recommended for each supply pin. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. 0.1- μ F and 1- μ F capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

11 Layout

11.1 Layout Guidelines

Reflections and matching are closely related to loop antenna theory, but different enough to warrant their own discussion. When a PCB trace turns a corner at a 90° angle, a reflection can occur. This is primarily due to the change of width of the trace. At the apex of the turn, the trace width is increased to 1.414 times its width. This upsets the transmission line characteristics, especially the distributed capacitance and self-inductance of the trace — resulting in the reflection. It is a given that not all PCB traces can be straight, and so they will have to turn corners. [Figure 13](#) shows progressively better techniques of rounding corners. Only the last example maintains constant trace width and minimizes reflections.

11.2 Layout Example

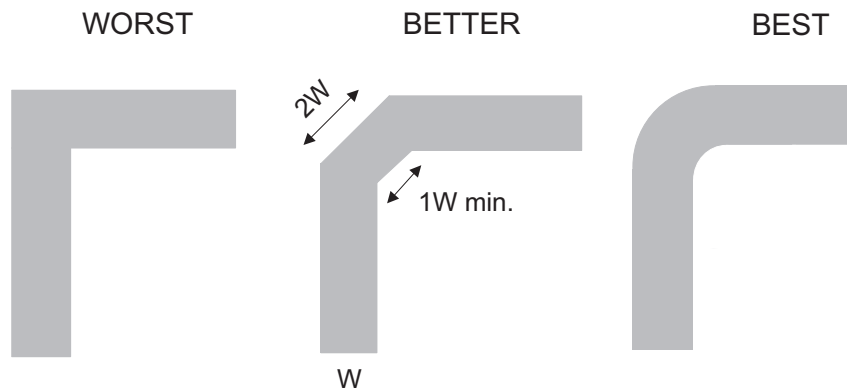


Figure 13. Trace Example

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

- *Implications of Slow or Floating CMOS Inputs*, [SCBA004](#)

12.2 Trademarks

NanoFree is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.3 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.4 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|-------------------|---------------|--------------|--------------------|------|----------------|----------------------------|----------------------------|----------------------|--------------|---|-------------------------|
| SN74LVC1G66DBVR | ACTIVE | SOT-23 | DBV | 5 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU CU SN | Level-1-260C-UNLIM | -40 to 85 | (C665, C66R, C66T) | Samples |
| SN74LVC1G66DBVRE4 | ACTIVE | SOT-23 | DBV | 5 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | (C665, C66R, C66T) | Samples |
| SN74LVC1G66DBVRG4 | ACTIVE | SOT-23 | DBV | 5 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | (C665, C66R, C66T) | Samples |
| SN74LVC1G66DBVT | ACTIVE | SOT-23 | DBV | 5 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU CU SN | Level-1-260C-UNLIM | -40 to 85 | (C665, C66R) | Samples |
| SN74LVC1G66DBVTG4 | ACTIVE | SOT-23 | DBV | 5 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | (C665, C66R) | Samples |
| SN74LVC1G66DCKR | ACTIVE | SC70 | DCK | 5 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU CU SN | Level-1-260C-UNLIM | -40 to 85 | (C65, C6F, C6J, C6 K, C6O, C6R, C 6T) | Samples |
| SN74LVC1G66DCKRE4 | ACTIVE | SC70 | DCK | 5 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | (C65, C6F, C6J, C6 K, C6O, C6R, C 6T) | Samples |
| SN74LVC1G66DCKRG4 | ACTIVE | SC70 | DCK | 5 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | (C65, C6F, C6J, C6 K, C6O, C6R, C 6T) | Samples |
| SN74LVC1G66DCKT | ACTIVE | SC70 | DCK | 5 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU CU SN | Level-1-260C-UNLIM | -40 to 85 | (C65, C6J, C6R, C6 T) | Samples |
| SN74LVC1G66DRLR | ACTIVE | SOT-5X3 | DRL | 5 | 4000 | Green (RoHS & no Sb/Br) | CU NIPDAU CU NIPDAUAG | Level-1-260C-UNLIM | -40 to 85 | (C67, C6R) | Samples |
| SN74LVC1G66DRLRG4 | ACTIVE | SOT-5X3 | DRL | 5 | 4000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | (C67, C6R) | Samples |
| SN74LVC1G66DRYR | ACTIVE | SON | DRY | 6 | 5000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | C6 | Samples |
| SN74LVC1G66DSF2 | ACTIVE | SON | DSF | 6 | 5000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | C6 | Samples |
| SN74LVC1G66DSFR | ACTIVE | SON | DSF | 6 | 5000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | C6 | Samples |
| SN74LVC1G66YZPR | ACTIVE | DSBGA | YZP | 5 | 3000 | Green (RoHS & no Sb/Br) | SNAGCU | Level-1-260C-UNLIM | -40 to 85 | C6N | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of ≤ 1000 ppm threshold. Antimony trioxide based flame retardants must also meet the ≤ 1000 ppm threshold requirement.

⁽³⁾ MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN74LVC1G66 :

- Automotive: [SN74LVC1G66-Q1](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74LVC1G66DBVR | SOT-23 | DBV | 5 | 3000 | 180.0 | 8.4 | 3.23 | 3.17 | 1.37 | 4.0 | 8.0 | Q3 |
| SN74LVC1G66DBVR | SOT-23 | DBV | 5 | 3000 | 178.0 | 9.2 | 3.3 | 3.23 | 1.55 | 4.0 | 8.0 | Q3 |
| SN74LVC1G66DBVR | SOT-23 | DBV | 5 | 3000 | 178.0 | 9.0 | 3.3 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| SN74LVC1G66DBVT | SOT-23 | DBV | 5 | 250 | 178.0 | 9.0 | 3.3 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| SN74LVC1G66DBVT | SOT-23 | DBV | 5 | 250 | 178.0 | 9.2 | 3.3 | 3.23 | 1.55 | 4.0 | 8.0 | Q3 |
| SN74LVC1G66DBVT | SOT-23 | DBV | 5 | 250 | 180.0 | 8.4 | 3.23 | 3.17 | 1.37 | 4.0 | 8.0 | Q3 |
| SN74LVC1G66DCKR | SC70 | DCK | 5 | 3000 | 178.0 | 9.2 | 2.4 | 2.4 | 1.22 | 4.0 | 8.0 | Q3 |
| SN74LVC1G66DCKR | SC70 | DCK | 5 | 3000 | 180.0 | 9.2 | 2.3 | 2.55 | 1.2 | 4.0 | 8.0 | Q3 |
| SN74LVC1G66DCKT | SC70 | DCK | 5 | 250 | 178.0 | 9.2 | 2.4 | 2.4 | 1.22 | 4.0 | 8.0 | Q3 |
| SN74LVC1G66DRLR | SOT-5X3 | DRL | 5 | 4000 | 180.0 | 8.4 | 1.98 | 1.78 | 0.69 | 4.0 | 8.0 | Q3 |
| SN74LVC1G66DRYR | SON | DRY | 6 | 5000 | 180.0 | 9.5 | 1.15 | 1.6 | 0.75 | 4.0 | 8.0 | Q1 |
| SN74LVC1G66DSF2 | SON | DSF | 6 | 5000 | 180.0 | 9.5 | 1.16 | 1.16 | 0.5 | 4.0 | 8.0 | Q3 |
| SN74LVC1G66DSFR | SON | DSF | 6 | 5000 | 180.0 | 9.5 | 1.16 | 1.16 | 0.5 | 4.0 | 8.0 | Q2 |
| SN74LVC1G66YZPR | DSBGA | YZP | 5 | 3000 | 178.0 | 9.2 | 1.02 | 1.52 | 0.63 | 4.0 | 8.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74LVC1G66DBVR | SOT-23 | DBV | 5 | 3000 | 202.0 | 201.0 | 28.0 |
| SN74LVC1G66DBVR | SOT-23 | DBV | 5 | 3000 | 180.0 | 180.0 | 18.0 |
| SN74LVC1G66DBVR | SOT-23 | DBV | 5 | 3000 | 180.0 | 180.0 | 18.0 |
| SN74LVC1G66DBVT | SOT-23 | DBV | 5 | 250 | 180.0 | 180.0 | 18.0 |
| SN74LVC1G66DBVT | SOT-23 | DBV | 5 | 250 | 180.0 | 180.0 | 18.0 |
| SN74LVC1G66DBVT | SOT-23 | DBV | 5 | 250 | 202.0 | 201.0 | 28.0 |
| SN74LVC1G66DCKR | SC70 | DCK | 5 | 3000 | 180.0 | 180.0 | 18.0 |
| SN74LVC1G66DCKR | SC70 | DCK | 5 | 3000 | 205.0 | 200.0 | 33.0 |
| SN74LVC1G66DCKT | SC70 | DCK | 5 | 250 | 180.0 | 180.0 | 18.0 |
| SN74LVC1G66DRLR | SOT-5X3 | DRL | 5 | 4000 | 202.0 | 201.0 | 28.0 |
| SN74LVC1G66DRYR | SON | DRY | 6 | 5000 | 184.0 | 184.0 | 19.0 |
| SN74LVC1G66DSF2 | SON | DSF | 6 | 5000 | 184.0 | 184.0 | 19.0 |
| SN74LVC1G66DSFR | SON | DSF | 6 | 5000 | 184.0 | 184.0 | 19.0 |
| SN74LVC1G66YZPR | DSBGA | YZP | 5 | 3000 | 220.0 | 220.0 | 35.0 |

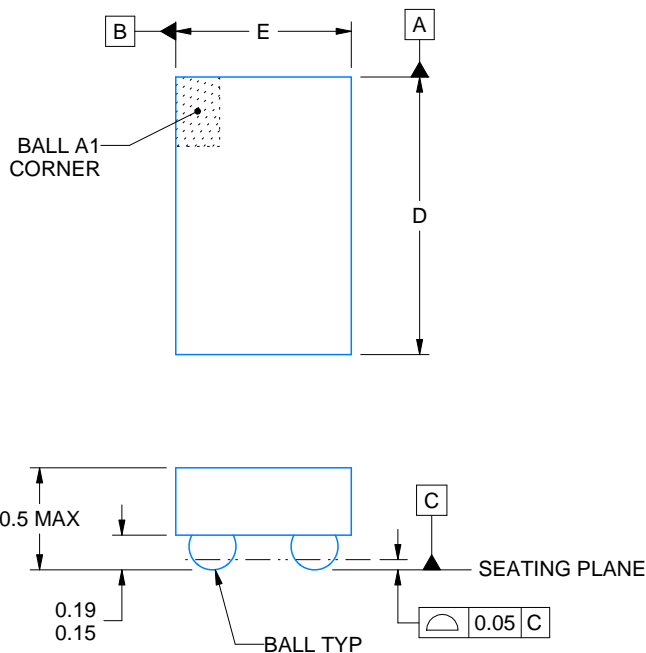
YZP0005



PACKAGE OUTLINE

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



D: Max = 1.418 mm, Min = 1.358 mm

E: Max = 0.918 mm, Min = 0.858 mm

4219492/A 05/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

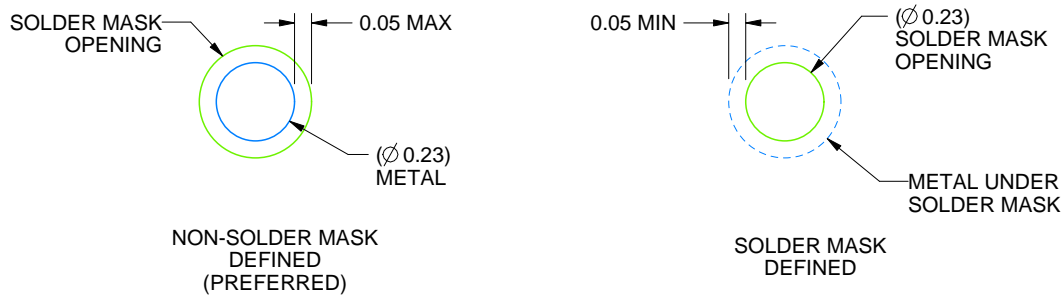
YZP0005

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE
SCALE:40X



SOLDER MASK DETAILS
NOT TO SCALE

4219492/A 05/2017

NOTES: (continued)

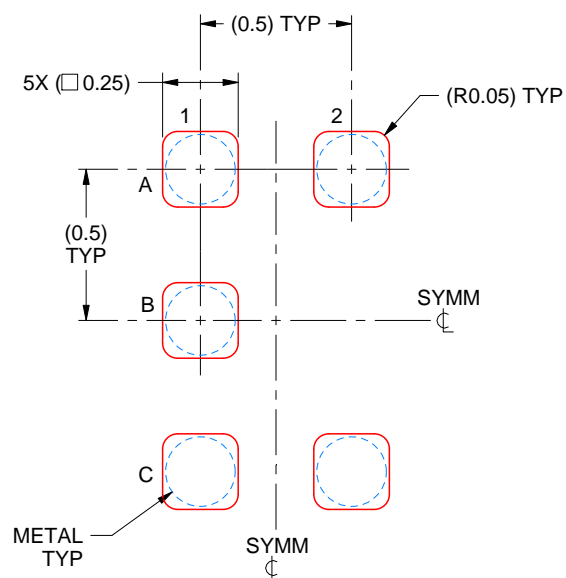
- Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).

EXAMPLE STENCIL DESIGN

YZP0005

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:40X

4219492/A 05/2017

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.



4205622-2/D 08/2007

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash, interlead flash, protrusions, or gate burrs. Mold flash, interlead flash, protrusions, or gate burrs shall not exceed 0,15 per end or side.
 - D. JEDEC package registration is pending.

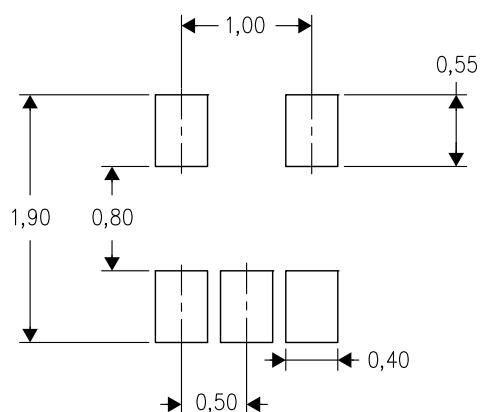
DRL (R-PDSO-N5)

PLASTIC SMALL OUTLINE

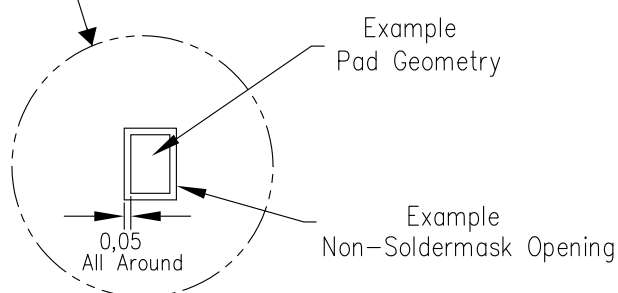
Example Board Layout



Example Stencil Design
(Note E)



Example
Non-Soldermask Defined Pad

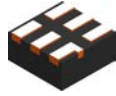


Example
Pad Geometry

Example
Non-Soldermask Opening

4208207-2/E 06/12

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
 - E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
 - F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - G. Side aperture dimensions over-print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

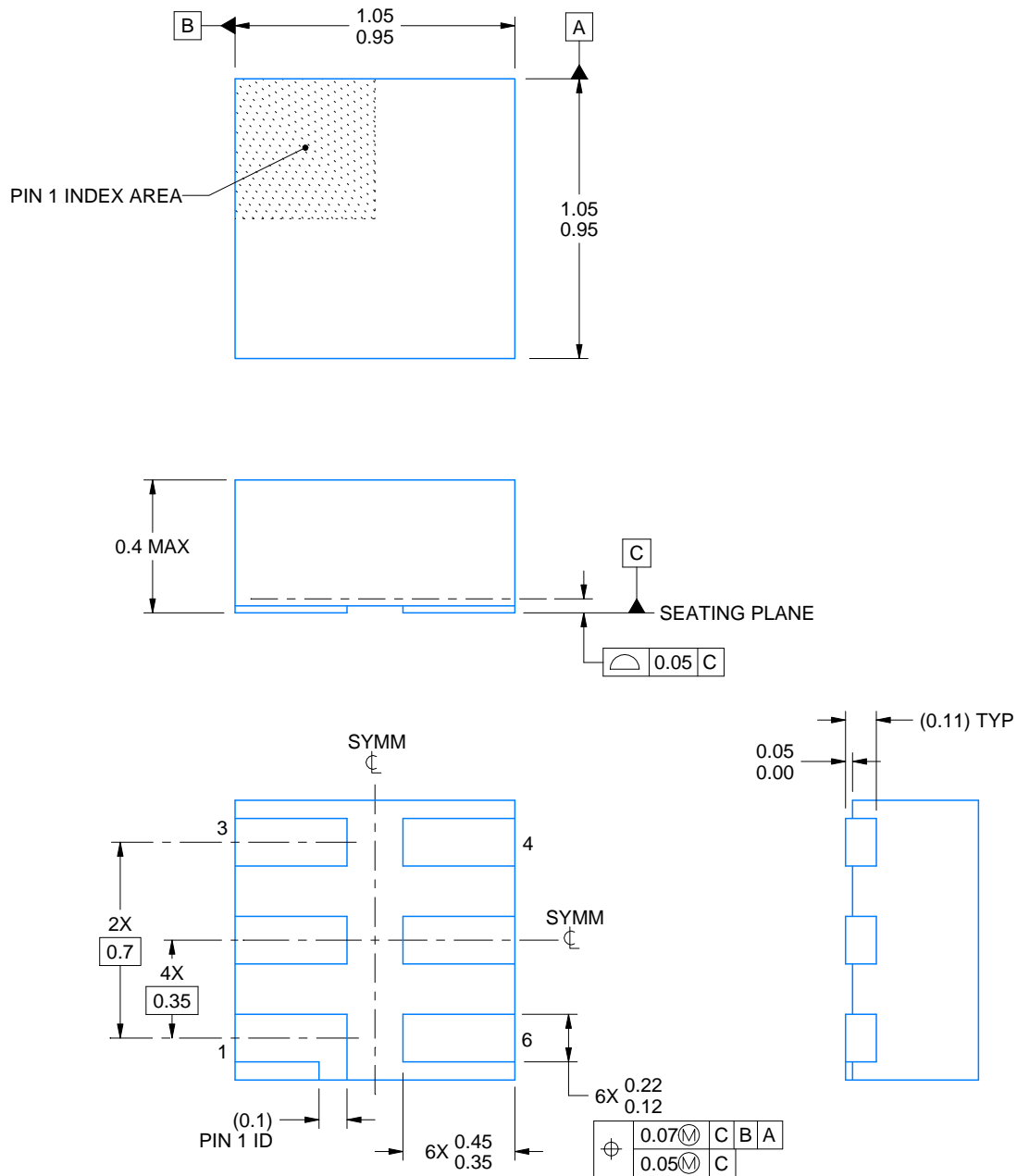


DSF0006A

PACKAGE OUTLINE

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



4220597/A 06/2017

NOTES:

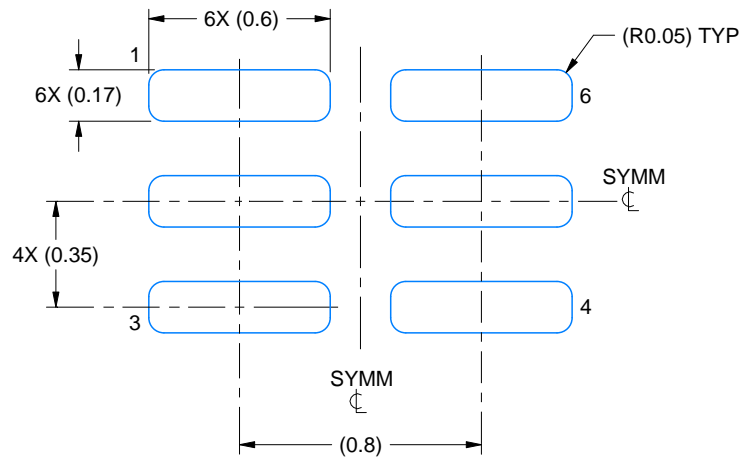
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration MO-287, variation X2AAF.

EXAMPLE BOARD LAYOUT

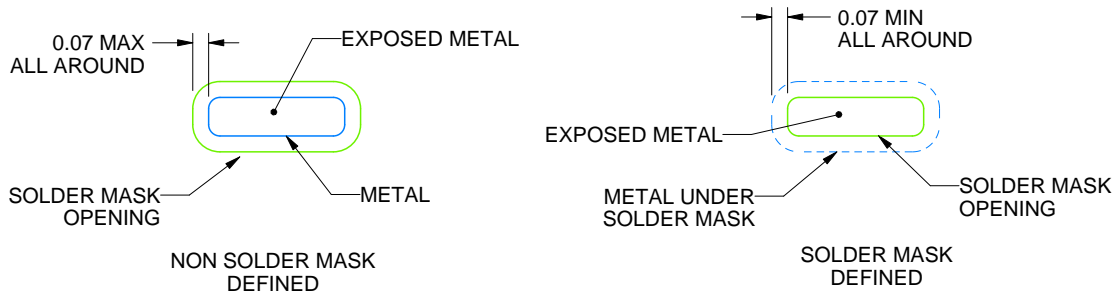
DSF0006A

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:40X



SOLDER MASK DETAILS

4220597/A 06/2017

NOTES: (continued)

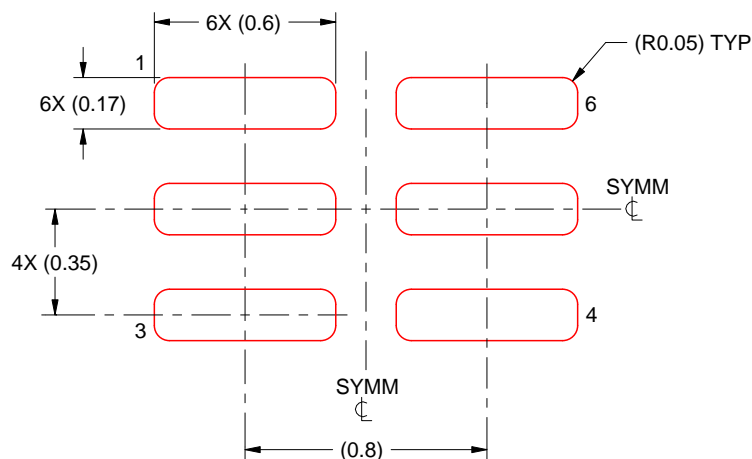
4. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

DSF0006A

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:40X

4220597/A 06/2017

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

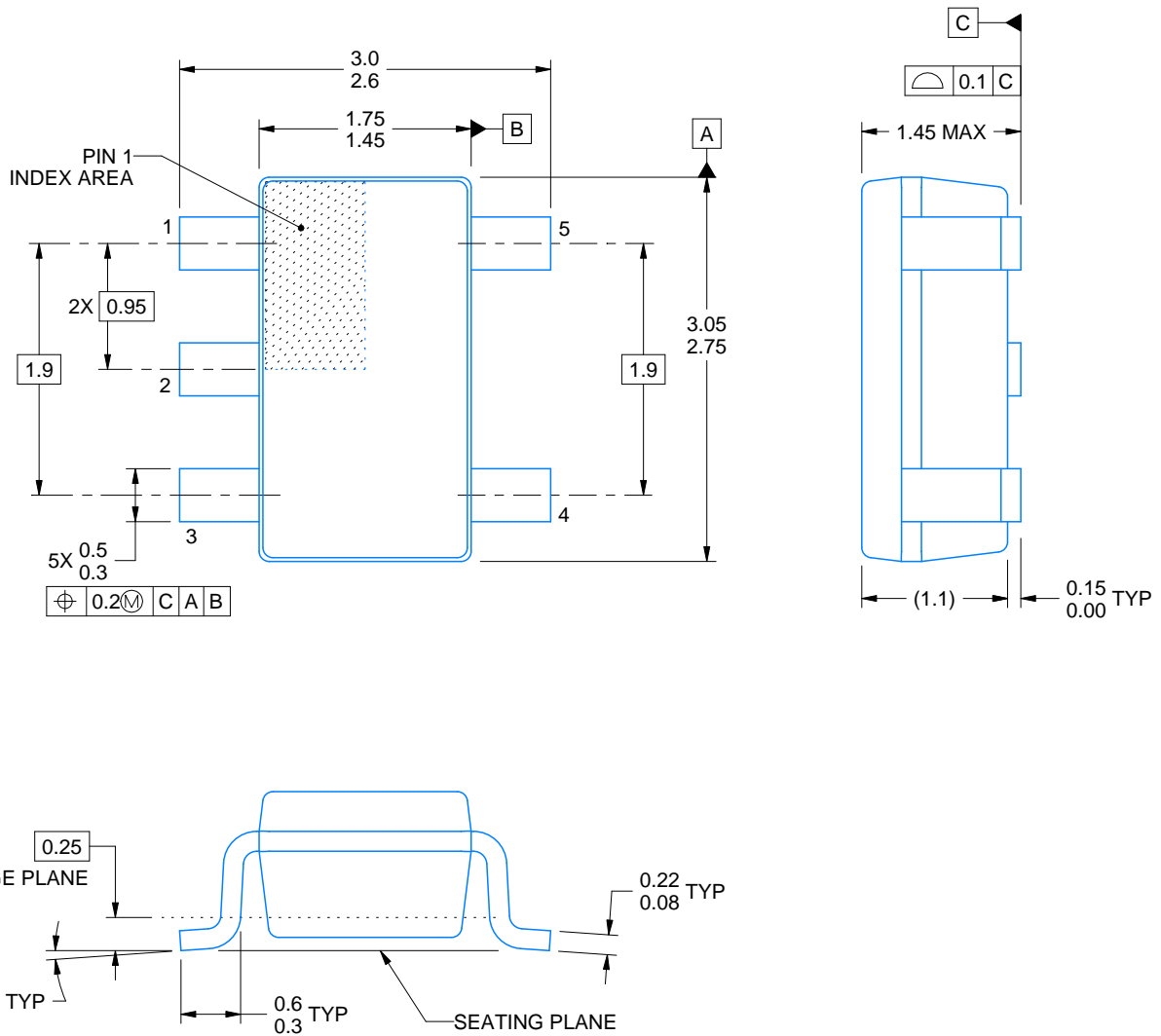
DBV0005A



PACKAGE OUTLINE

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



4214839/D 11/2018

NOTES:

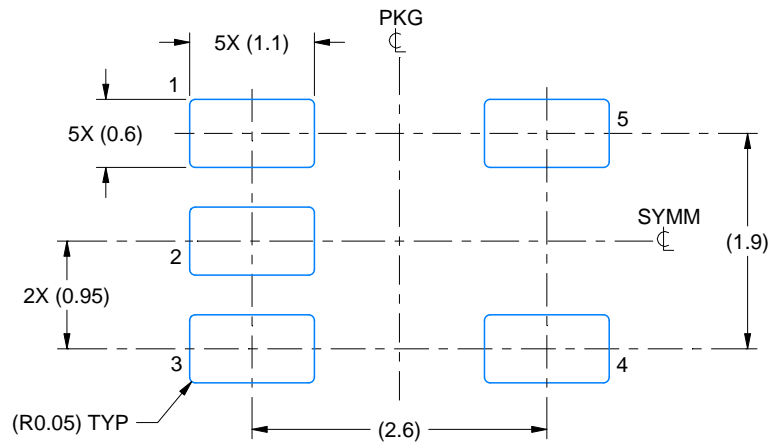
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.

EXAMPLE BOARD LAYOUT

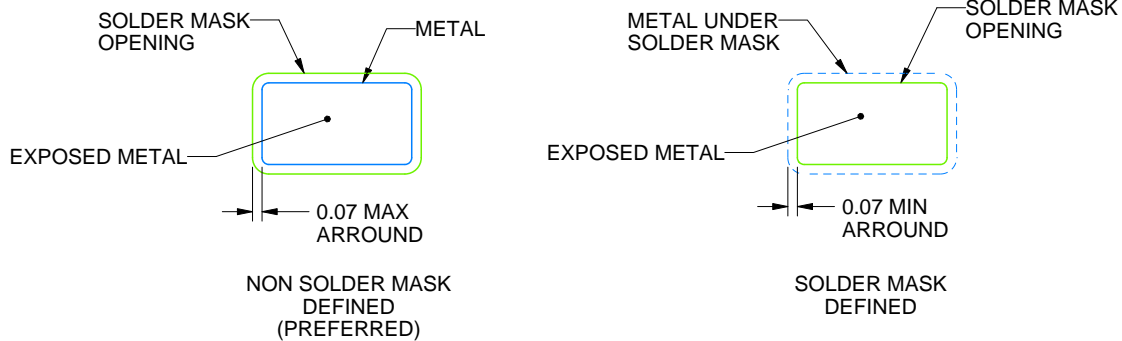
DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4214839/D 11/2018

NOTES: (continued)

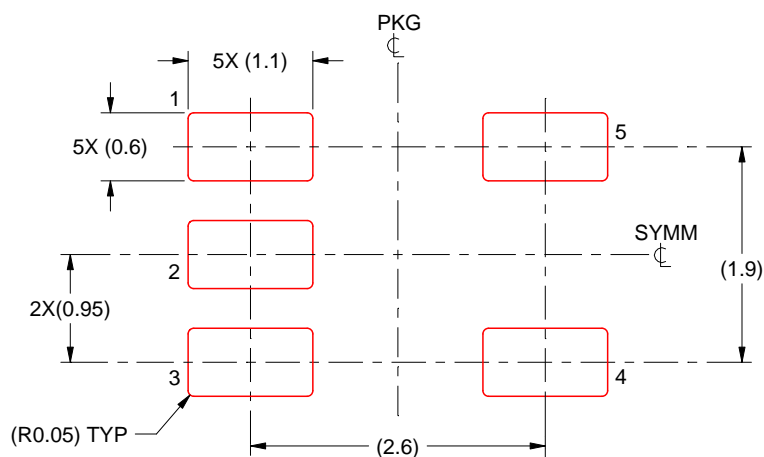
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/D 11/2018

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

DCK (R-PDSO-G5)

PLASTIC SMALL-OUTLINE PACKAGE



4093553-3/G 01/2007

- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
 - Falls within JEDEC MO-203 variation AA.

DCK (R-PDSO-G5)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
 - D. Publication IPC-7351 is recommended for alternate designs.
 - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

GENERIC PACKAGE VIEW

DRY 6

USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4207181/G



USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



4222894/A 01/2018

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

DRY0006A

USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
1:1 RATIO WITH PKG SOLDER PADS
EXPOSED METAL SHOWN
SCALE:40X



SOLDER MASK DETAILS

4222894/A 01/2018

NOTES: (continued)

3. For more information, see QFN/SON PCB application report in literature No. SLUA271 (www.ti.com/lit/slue271).

EXAMPLE STENCIL DESIGN

DRY0006A

USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.075 - 0.1 mm THICK STENCIL
SCALE:40X

4222894/A 01/2018

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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