

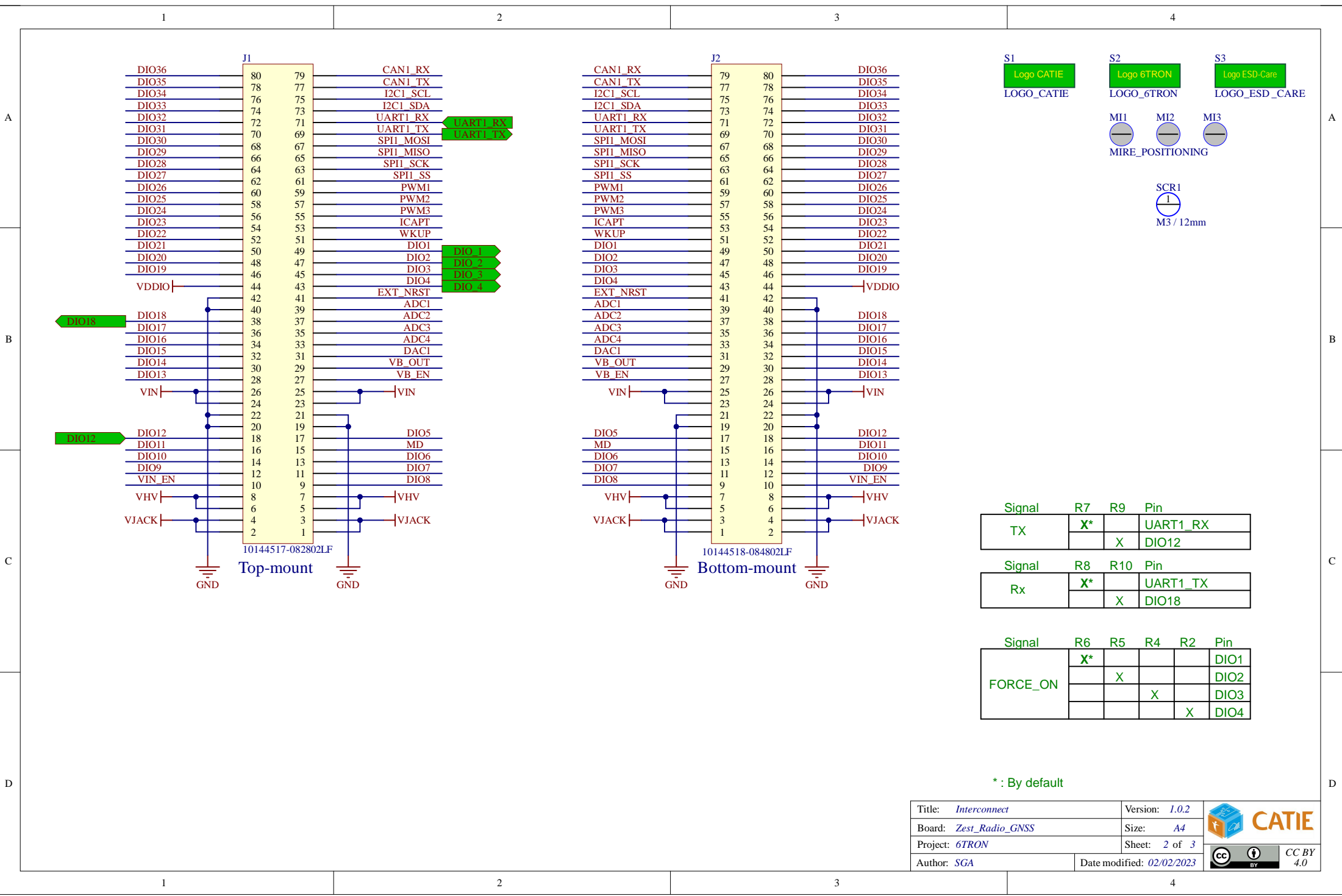


Title: <i>Block Diagram</i>	Version: <i>1.0.2</i>	
Board: <i>Zest_Radio_GNSS</i>	Size: <i>A4</i>	
Project: <i>6TRON</i>	Sheet: <i>1 of 3</i>	
Author: <i>SGA</i>	Date modified: <i>02/02/2023</i>	



Signal	R7	R9	Pin
TX	X*		UART1_RX
		X	DIO12

Signal	R8	R10	Pin
Rx	X*		UART1_TX
		X	DIO18

Signal	R6	R5	R4	R2	Pin
FORCE_ON	X*				DIO1
		X			DIO2
			X		DIO3
				X	DIO4

\* : By default

Title: <i>Interconnect</i>	Version: <i>1.0.2</i>	
Board: <i>Zest_Radio_GNSS</i>	Size: <i>A4</i>	
Project: <i>6TRON</i>	Sheet: <i>2 of 3</i>	
Author: <i>SGA</i>	Date modified: <i>02/02/2023</i>	

A

B

C

D

A

B

C

D

1

2

3

4

1

2

3

4

