

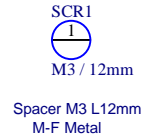
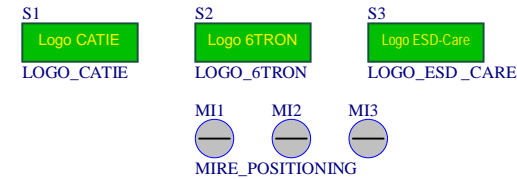
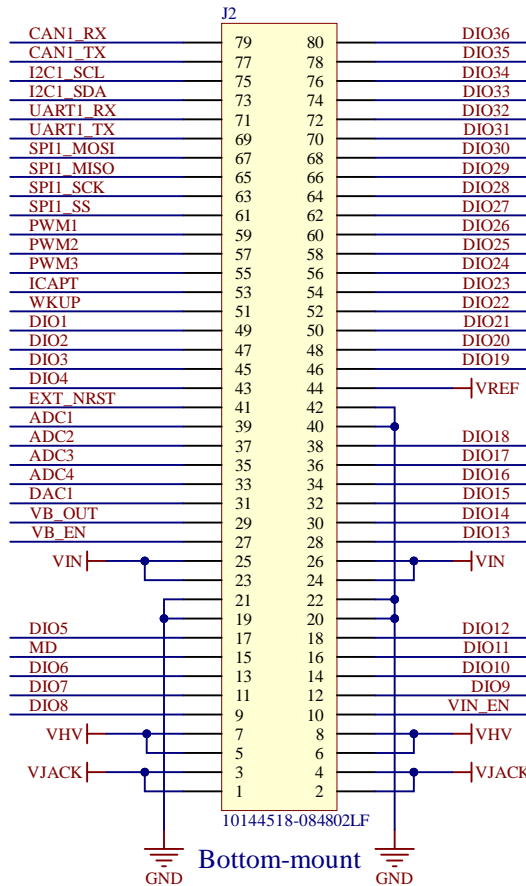
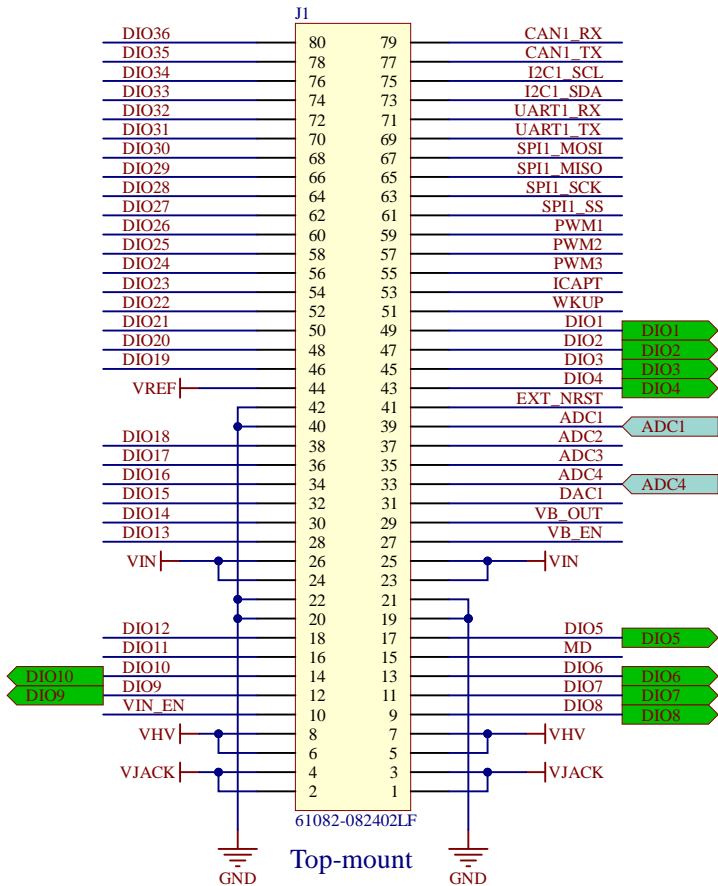


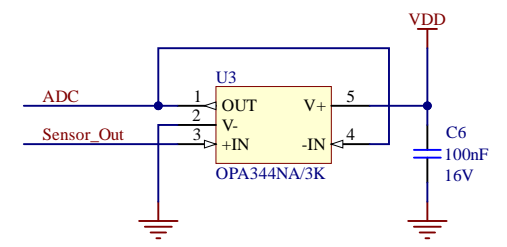
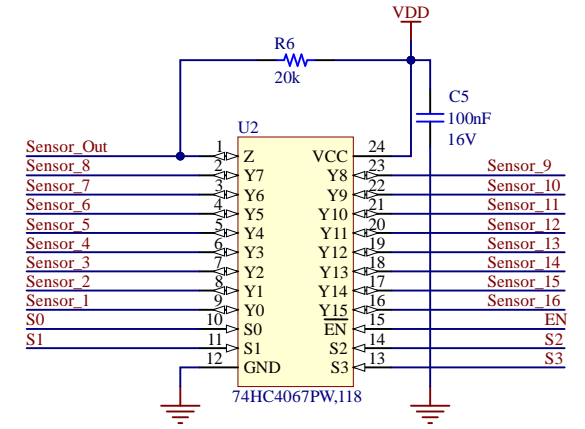
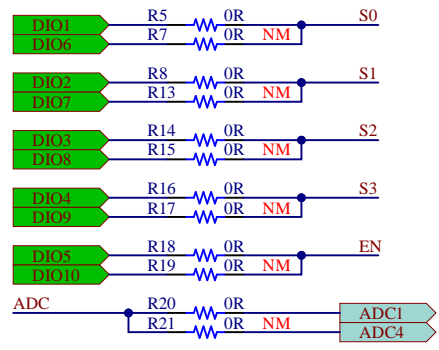
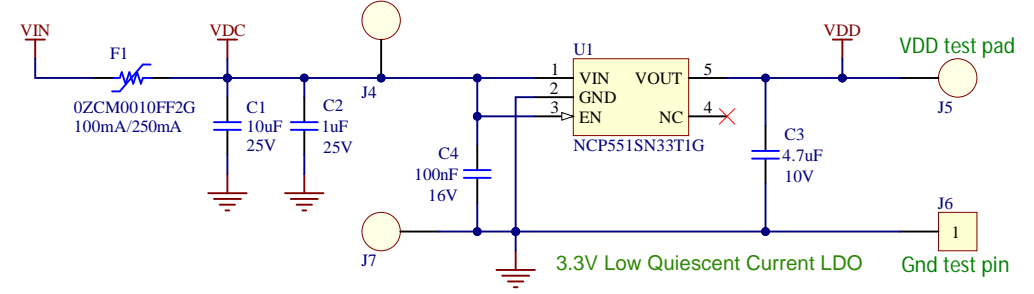
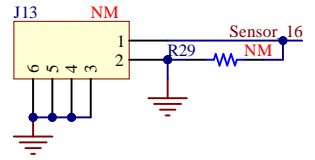
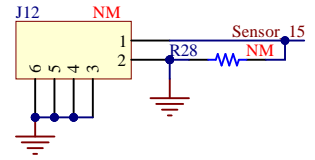
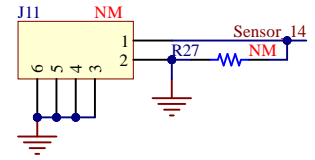
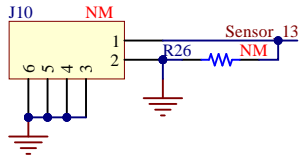
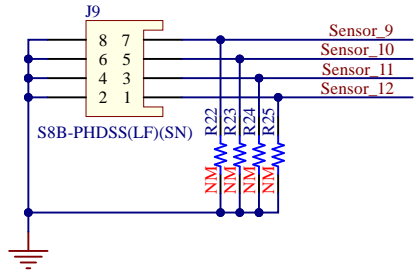
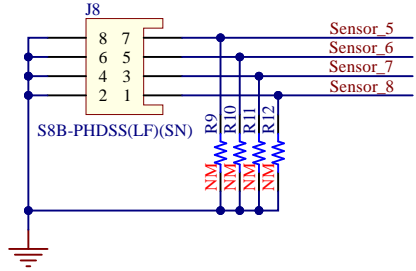
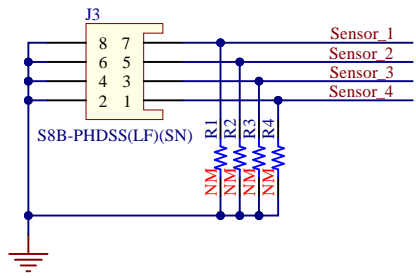
Title: <i>Block Diagram</i>	Version: <i>1.0.0</i>	
Board: <i>Zest_Interface_AnalogMux</i>	Size: <i>A4</i>	
Project: <i>6TRON</i>	Sheet: <i>1 of 3</i>	
Author: <i>SGA</i>	Date modified: <i>01/03/2023</i>	



Signal	R5	R7	Pin
S0	X*		DIO1
		X	DIO6
Signal	R8	R13	Pin
S1	X*		DIO2
		X	DIO7
Signal	R14	R15	Pin
S2	X*		DIO3
		X	DIO8
Signal	R16	R17	Pin
S3	X*		DIO4
		X	DIO9
Signal	R18	R19	Pin
EN	X*		DIO5
		X	DIO10
Signal	R20	R21	Pin
ADC	X*		ADC1
		X	ADC4

* : By default

Title: <i>Interconnect</i>	Version: <i>1.0.0</i>	
Board: <i>Zest_Interface_AnalogMux</i>	Size: <i>A4</i>	
Project: <i>6TRON</i>	Sheet: <i>2 of 3</i>	
Author: <i>SGA</i>	Date modified: <i>06/03/2023</i>	



Title: Control	Version: 1.0.0	
Board: Zest_Interface_AnalogMux	Size: A4	
Project: 6TRON	Sheet: 3 of 3	
Author: SGA	Date modified: 06/03/2023	

