

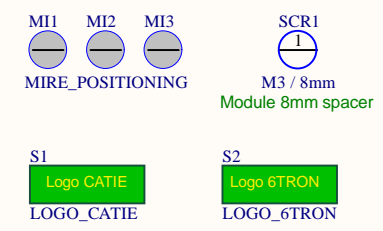
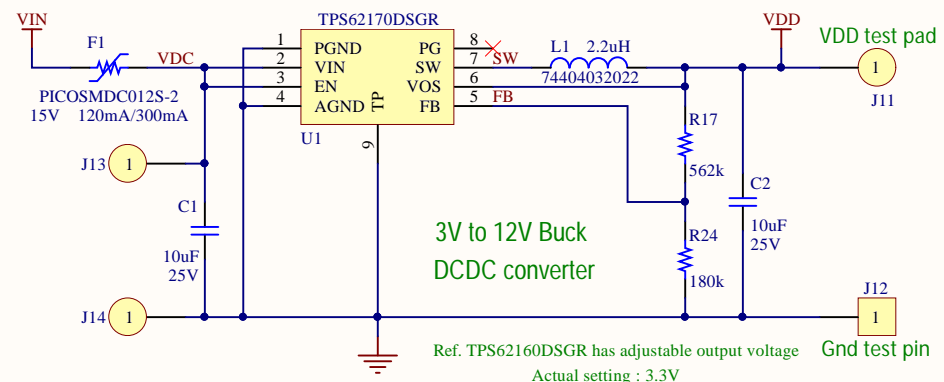
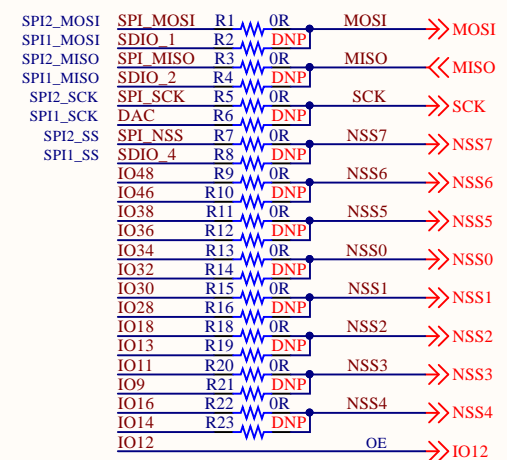
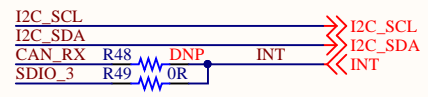
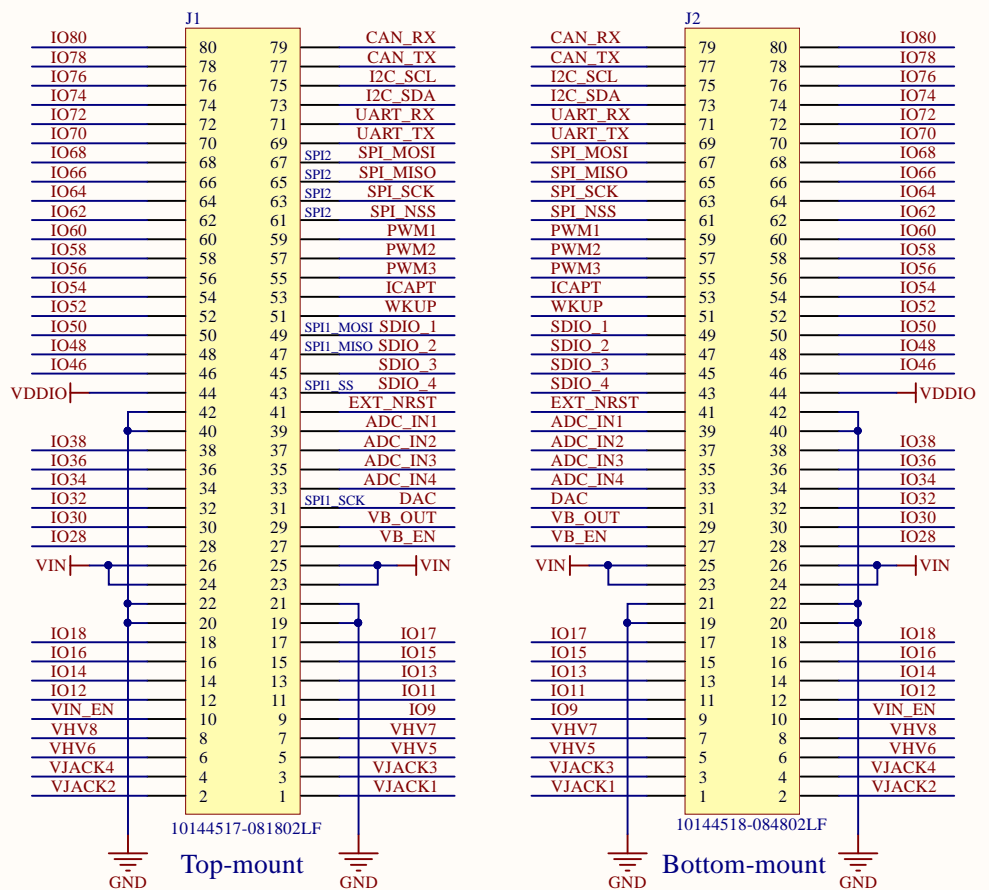
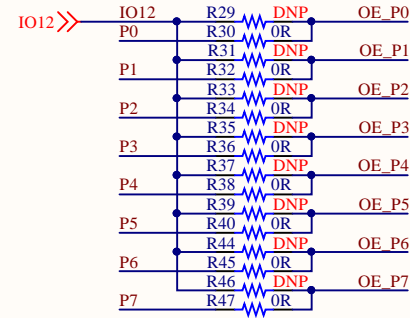
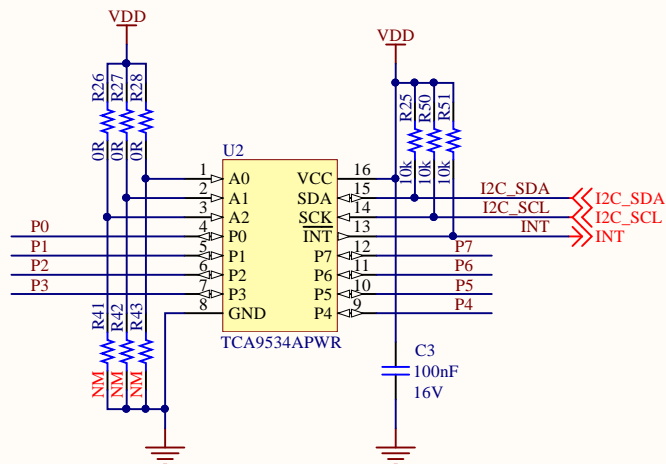
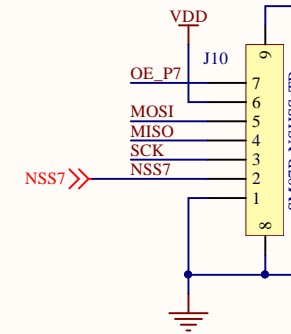
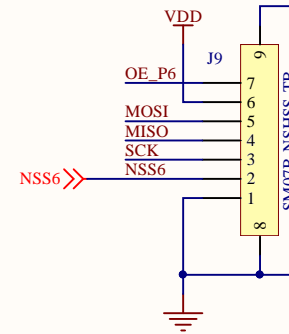
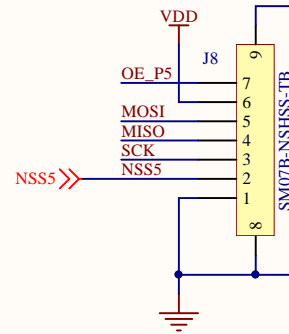
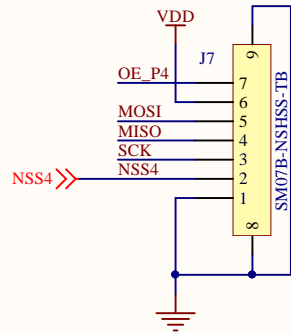
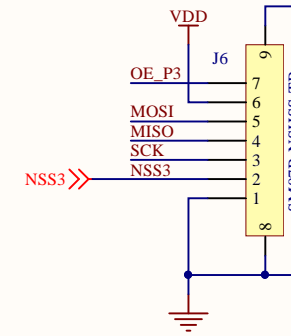
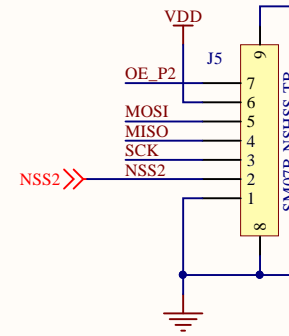
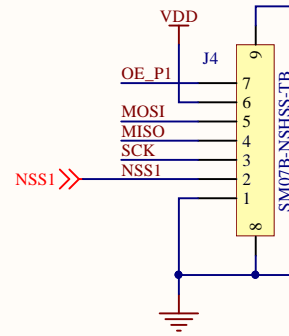
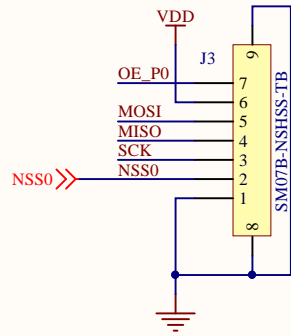


Title: <i>Synoptic</i>	Version: <i>1.1.0</i>	 CATIE <small>Solutions pour le secteur numérique</small>
Board: <i>Zest_Extension_SPI</i>	Size: <i>A4</i>	
Project: <i>6TRON</i>	Sheet: <i>1 of 3</i>	 CC BY 4.0
Author: <i>OC</i>	Date modified: <i>08/12/2019</i>	



Title: <i>Interface</i>	Version: <i>1.1.0</i>	
Board: <i>Zest_Extension_SPI</i>	Size: <i>A4</i>	
Project: <i>6TRON</i>	Sheet: <i>2 of 3</i>	
Author: <i>OC</i>	Date modified: <i>08/12/2019</i>	





Title: <i>Interconnect</i>	Version: <i>1.1.0</i>	
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