

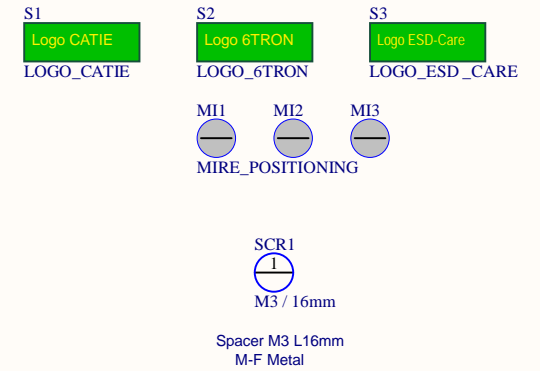
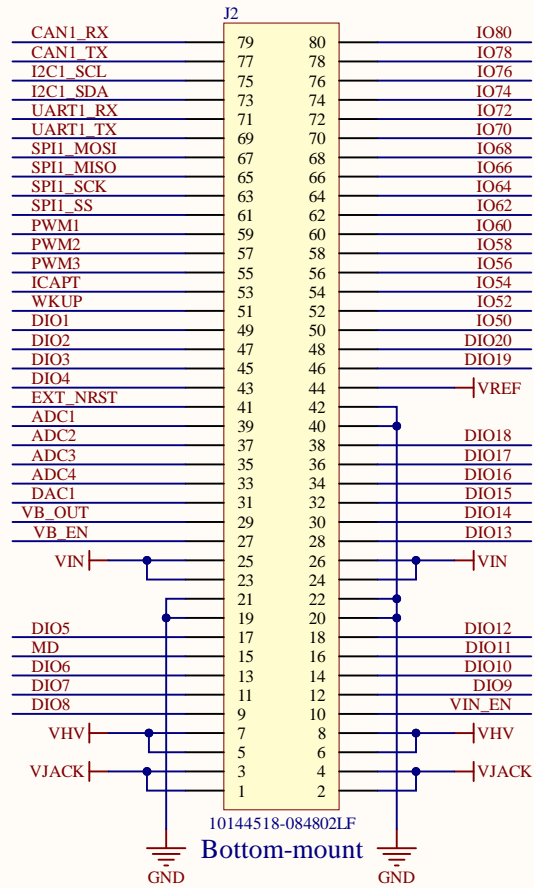
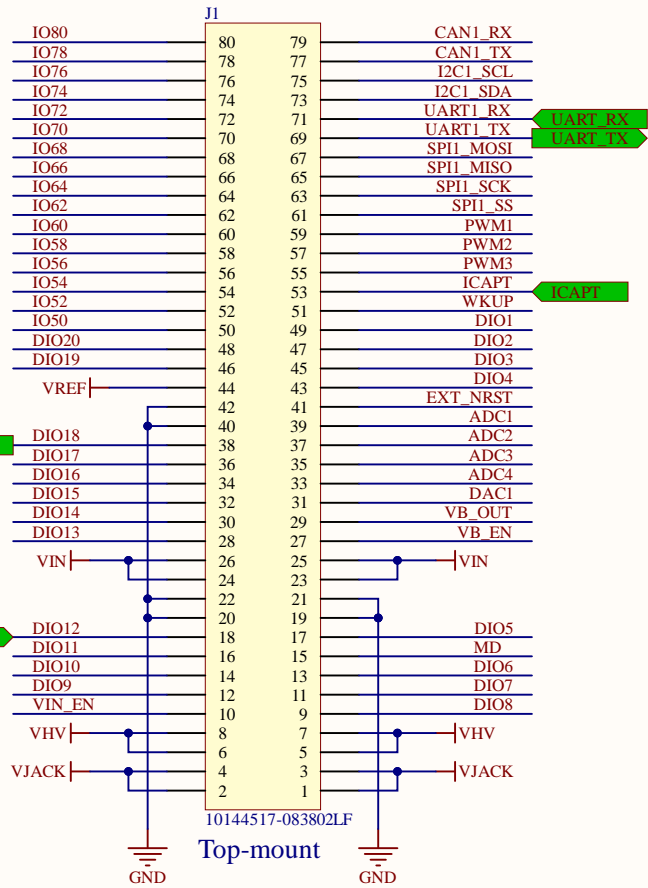


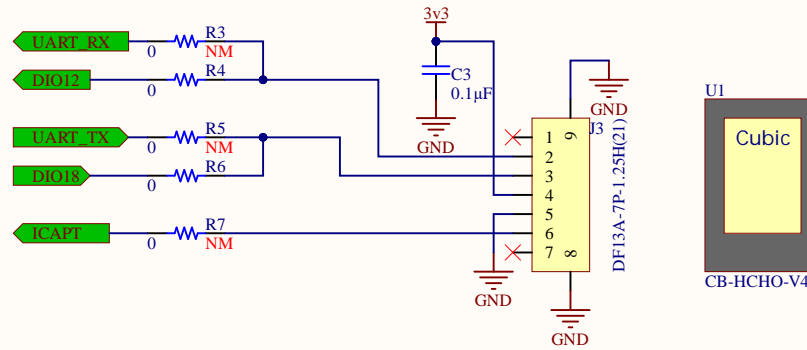
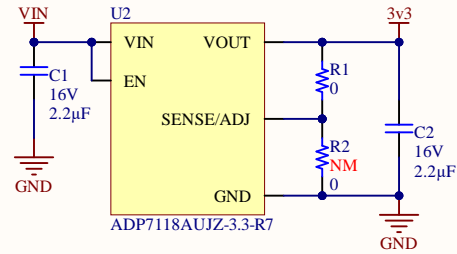
Title: <i>Block Diagram</i>	Version: <i>1.1.0</i>	
Board: <i>Zest_Sensor_VOC</i>	Size: <i>A4</i>	
Project: <i>6TRON</i>	Sheet: <i>1 of 3</i>	
Author: <i>SGA</i>	Date modified: <i>24/12/2021</i>	





Signal	R5	R6	Pin
UART_TX	X		UART_TX
		X*	DIO18
Signal	R3	R4	Pin
UART_RX	X		UART_RX
		X*	DIO12

\* : By default

Title: <i>Interconnect</i>	Version: <i>1.1.0</i>	
Board: <i>Zest_Sensor_VOC</i>	Size: <i>A4</i>	
Project: <i>6TRON</i>	Sheet: <i>2 of 3</i>	
Author: <i>SGA</i>	Date modified: <i>28/12/2021</i>	



Title: <i>Sensor</i>	Version: <i>1.1.0</i>	
Board: <i>Zest_Sensor_VOC</i>	Size: <i>A4</i>	
Project: <i>6TRON</i>	Sheet: <i>3 of 3</i>	
Author: <i>SGA</i>	Date modified: <i>04/01/2022</i>	