

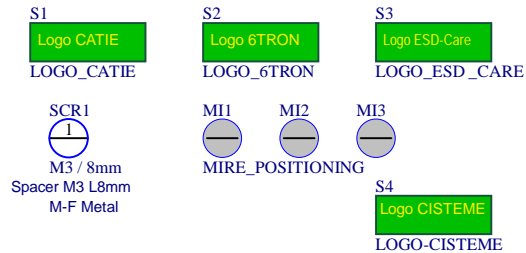
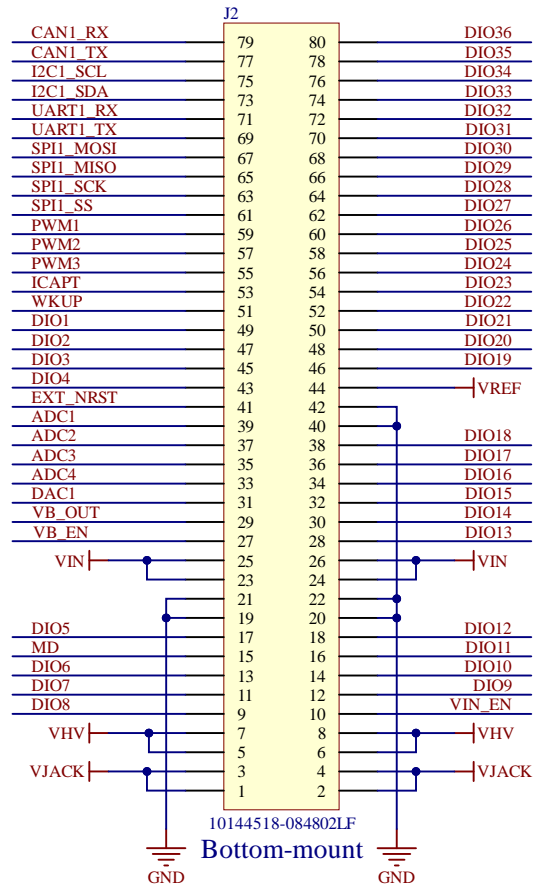
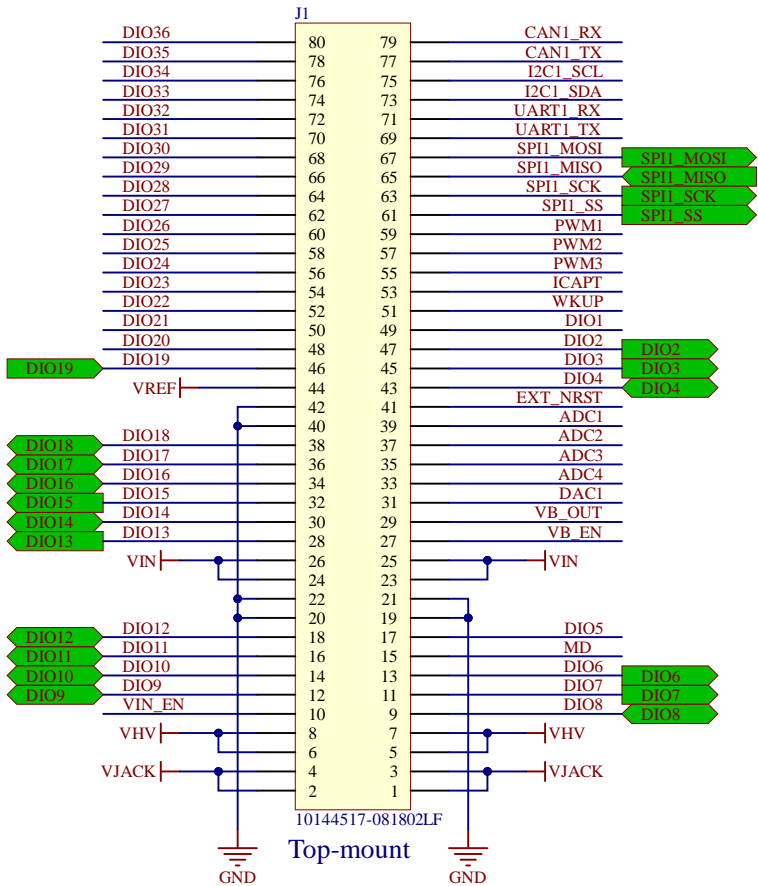


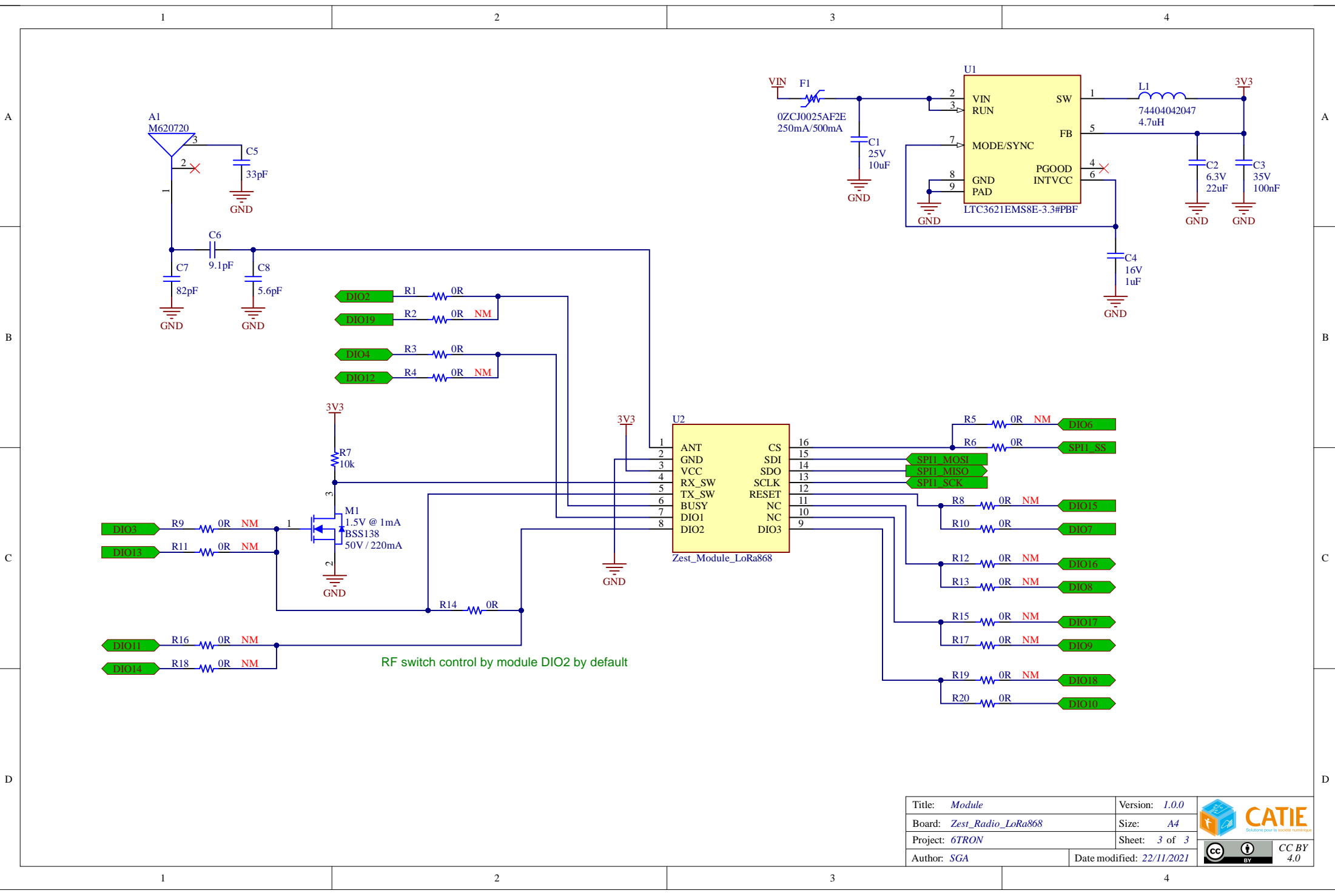
Title: <i>Block Diagram</i>	Version: <i>1.0.0</i>	
Board: <i>Zest_Radio_LoRa868</i>	Size: <i>A4</i>	
Project: <i>6TRON</i>	Sheet: <i>1 of 3</i>	
Author: <i>SGA</i>	Date modified: <i>22/11/2021</i>	



Signal	R6	R5	Pin
CS	X*		SPI1_SS DIO6
BUSY	X*	X	DIO2 DIO19
DIO1	X*	X	DIO4 DIO12
DIO2	X*	X	TX_SW DIO11 DIO14
TX_SW	X*	X	DIO2 DIO3 DIO13
DIO3	X*	X	DIO10 DIO18
DIO4	X	X	DIO9 DIO17
DIO5	X	X	DIO8 DIO16
RESET	X*	X	DIO7 DIO15

* : By default

Title: <i>Interconnect</i>	Version: <i>1.0.0</i>	
Board: <i>Zest_Radio_LoRa868</i>	Size: <i>A4</i>	
Project: <i>6TRON</i>	Sheet: <i>2 of 3</i>	
Author: <i>SGA</i>	Date modified: <i>26/01/2022</i>	



RF switch control by module DIO2 by default

Title: <i>Module</i>	Version: <i>1.0.0</i>	
Board: <i>Zest_Radio_LoRa868</i>	Size: <i>A4</i>	
Project: <i>6TRON</i>	Sheet: <i>3 of 3</i>	
Author: <i>SGA</i>	Date modified: <i>22/11/2021</i>	

