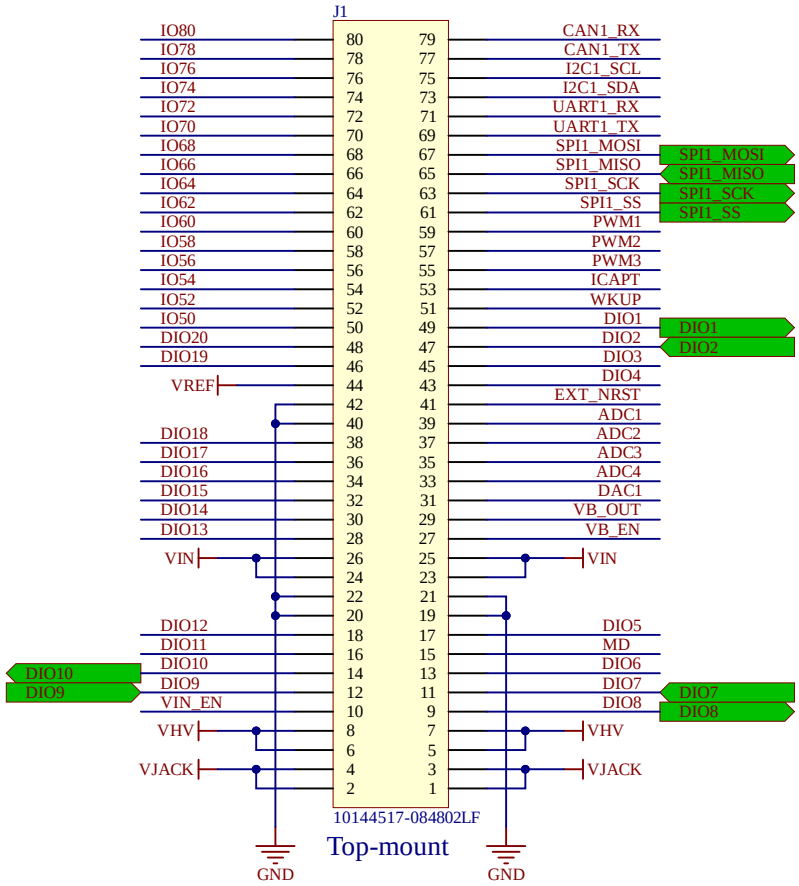
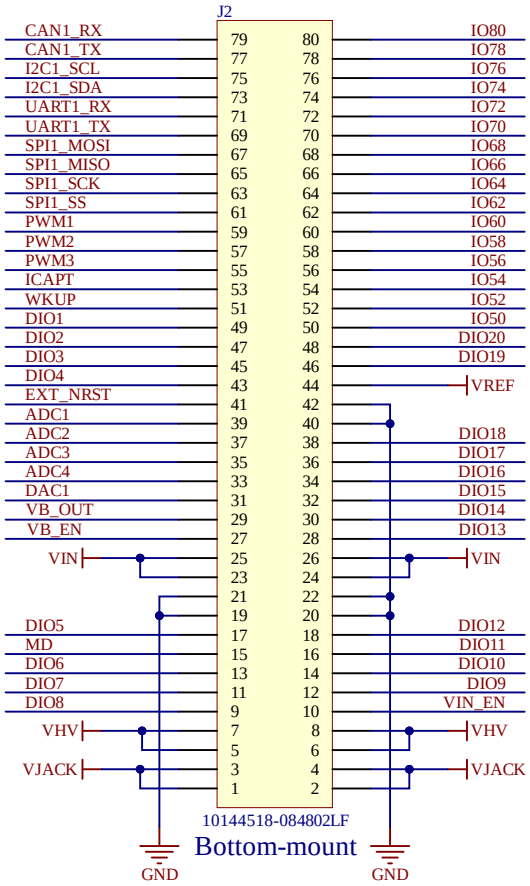
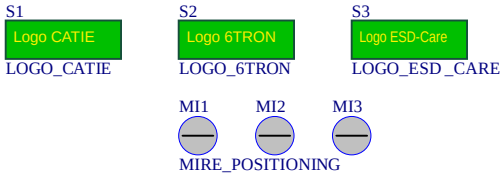
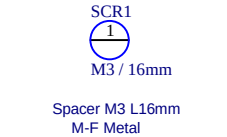






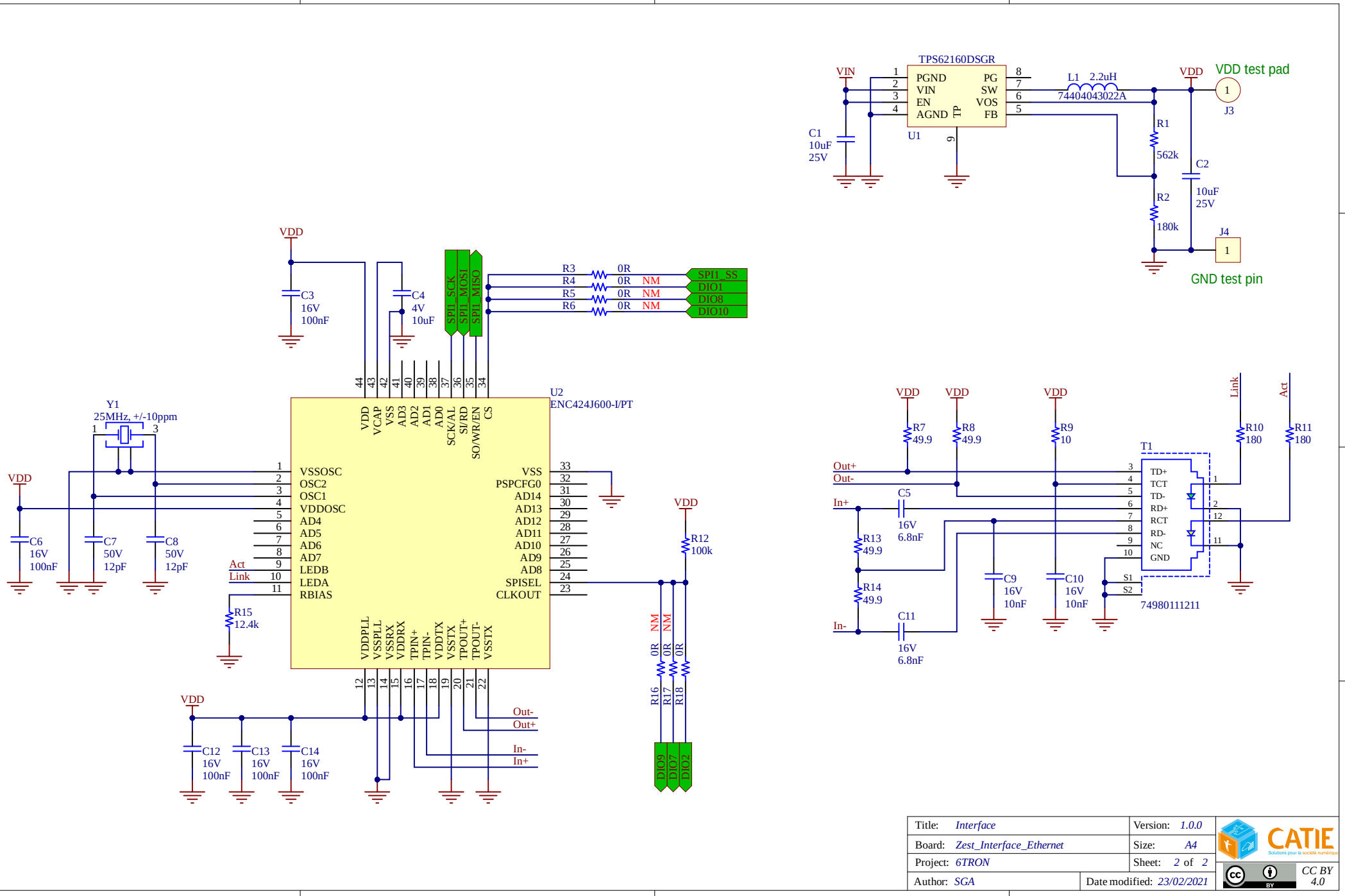


Signal	R3	R4	R5	R6	Pin
CS	X*				SPI1_SS
		X			DIO1
			X		DIO8
				X	DIO10

Signal	R18	R17	R16	Pin
SPI_INT	X*			DIO2
		X		DIO7
			X	DIO9

* : By default

Title: *Interconnect*		Version: *1.0.0*	
Board: *Zest_Interface_Ethernet*		Size: *A4*	
Project: *6TRON*		Sheet: *1* of *2*	
Author: *SGA*	Date modified: *20/11/2020*		



Title: *Interface*		Version: *1.0.0*	
Board: *Zest_Interface_Ethernet*		Size: *A4*	
Project: *6TRON*		Sheet: *2 of 2*	
Author: *SGA*	Date modified: *23/02/2021*		