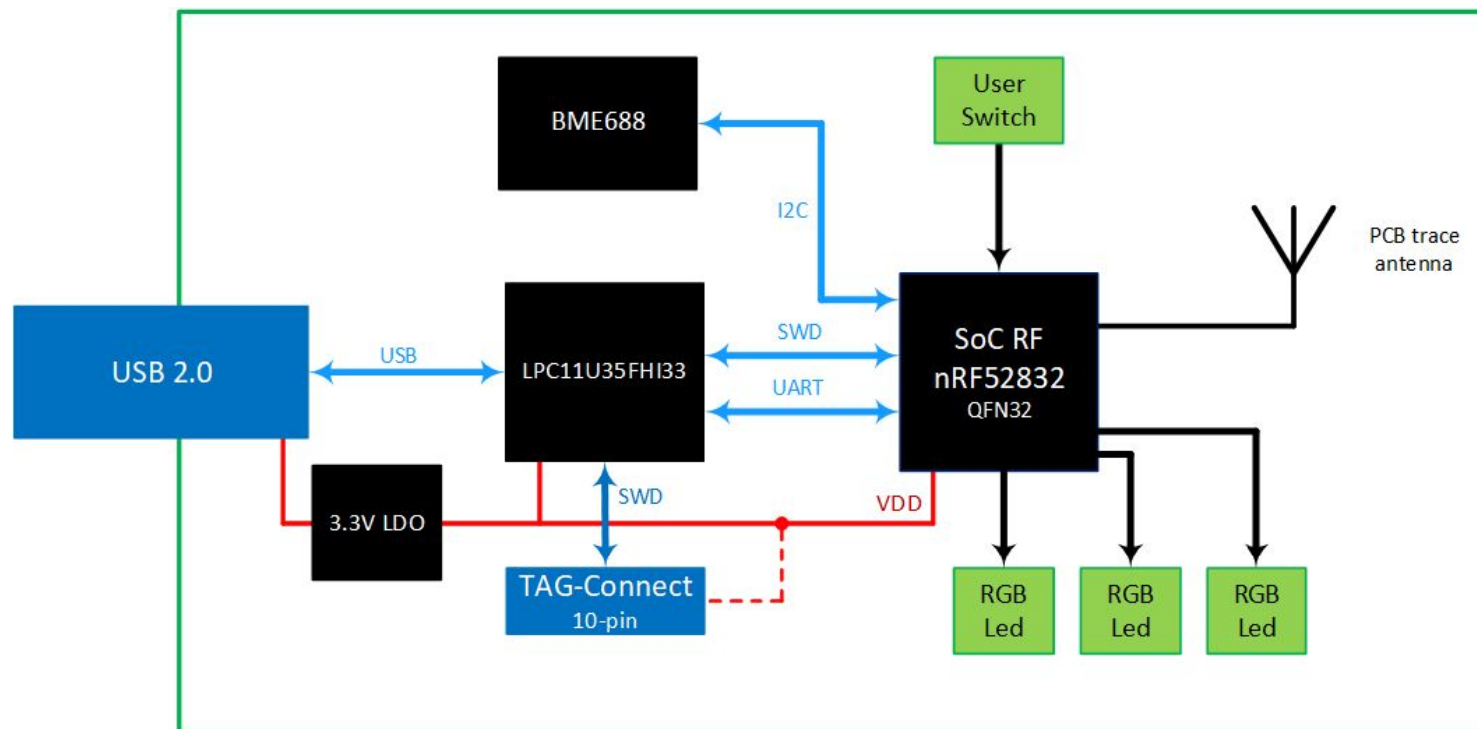
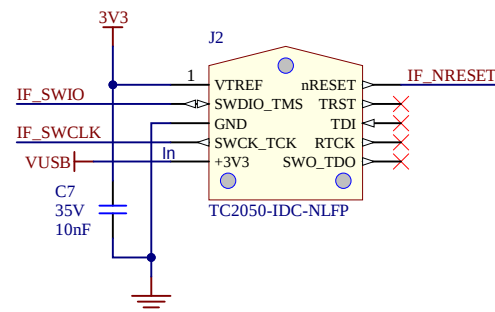
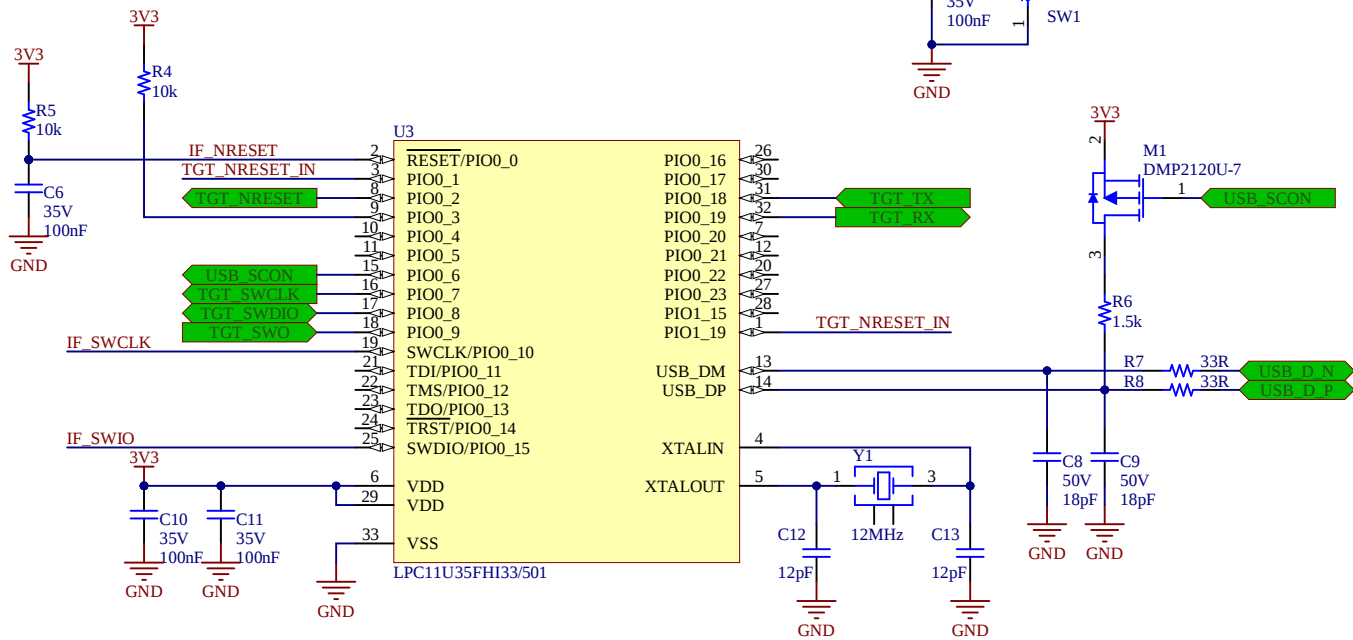
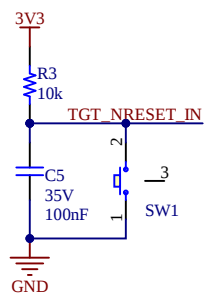
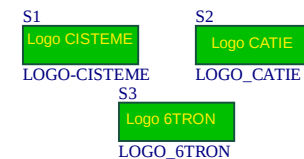
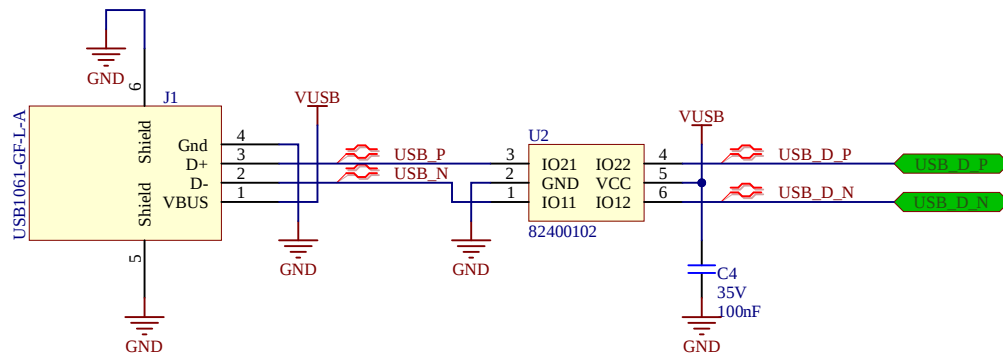
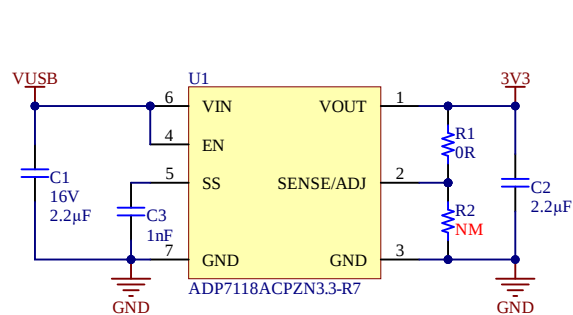
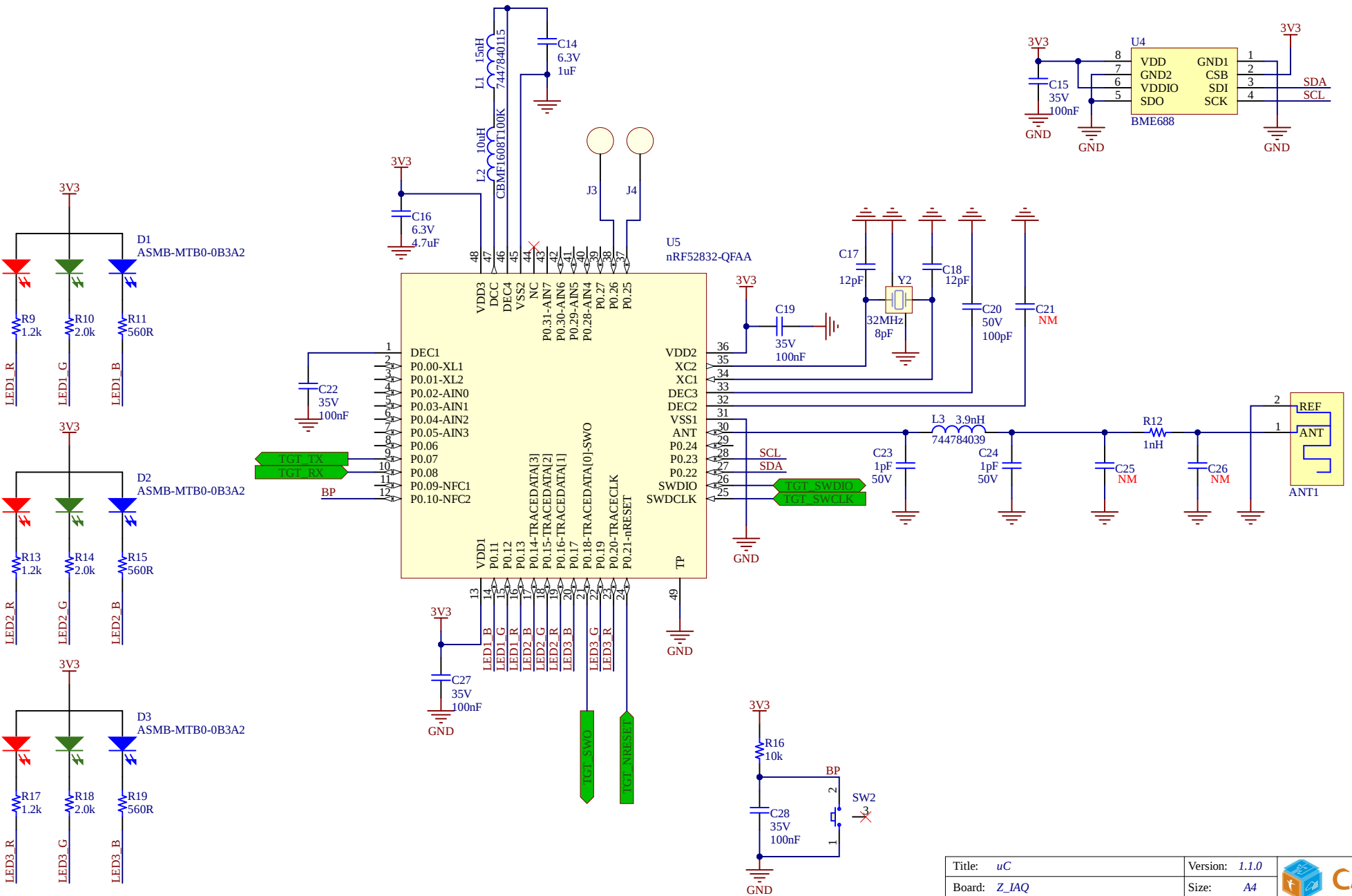






Title: <i>Interconnect</i>	Version: <i>1.1.0</i>	
Board: <i>Z_JAQ</i>	Size: <i>A4</i>	
Project: <i>CATIE</i>	Sheet: <i>2 of 3</i>	
Author: <i>SGA</i>	Date modified: <i>05/10/2022</i>	
		



Title: uC	Version: 1.1.0	
Board: Z_JAQ	Size: A4	
Project: CATIE	Sheet: 3 of 3	
Author: SGA	Date modified: 05/10/2022	

